# Design and Physical Implementation of a 1024 Point Fixed Point FFT Processor

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***Abstract*—This report presents the design, verification, synthesis, and physical implementation of a 1024 point fixed point fast Fourier transform processor. The design uses a radix 2 decimation in time FFT structure, Q1.15 fixed point arithmetic, a reusable butterfly processing element, a twiddle factor ROM, and a dual SRAM bank memory organization. The architecture was verified against a Python floating point reference model and then implemented through a standard ASIC backend flow using Design Compiler, PrimeTime, and Cadence Innovus. Post implementation simulation of the APR netlist produced an RMSE of $3.797 \times 10^{-5}$ and an RMS normalized error of $1.161 \times 10^{-2}$ relative to the floating point reference. Post layout timing analysis at a 10 ns clock period showed no setup or hold timing violations, with 5.48 ns setup slack and 0.19 ns hold slack in the clocked path group. The final implementation generated DEF, GDS, SPEF, SDF, and routed netlist outputs.**

## I. Introduction

The fast Fourier transform is a fundamental computation in digital signal processing systems. Hardware FFT processors are commonly used when high throughput and deterministic latency are required. This project implements a 1024 point FFT processor as an ASIC oriented design. The main goals are to develop a synthesizable RTL architecture, verify the numerical accuracy of the fixed point implementation, integrate generated SRAM macros, and complete a backend implementation flow including synthesis, placement, routing, and static timing analysis.

The implemented design follows a radix 2 decimation in time algorithm. A single butterfly processing element is reused over all stages to reduce logic area. Intermediate values are stored in two 1024 by 32 bit SRAM banks, where each word contains a signed 16 bit real component and a signed 16 bit imaginary component. The processor uses per stage right shift scaling to control numerical growth and produces an output equivalent to a scaled FFT, $X[k]/1024$.

## II. FFT Algorithm and Fixed Point Format

The $N$ point DFT is defined as

$$X[k] = \sum_{n=0}^{N-1} x[n] W_N^{nk}, \qquad W_N = e^{-j2\pi/N}. \tag{1}$$

For $N = 1024$, the radix 2 FFT has $\log_2(1024) = 10$ stages. Each butterfly computes

$$Y_0 = (A + BW) \gg 1, \tag{2}$$

$$Y_1 = (A - BW) \gg 1, \tag{3}$$

where $A$ and $B$ are complex inputs, $W$ is the twiddle factor, and the arithmetic right shift implements per stage normalization. Since a right shift is applied in each of the 10 stages, the final output is scaled by $1/1024$.

All datapath values use Q1.15 fixed point format. A complex data word is stored as a 32 bit value, with the upper 16 bits representing the real part and the lower 16 bits representing the imaginary part. The complex multiplier multiplies Q1.15 operands and shifts the intermediate products back to Q1.15 format.

## III. System Architecture

Fig. 1 shows the top level datapath. The architecture consists of a controller, twiddle ROM, two SRAM banks, operand registers, butterfly PE, and writeback mux. The testbench access path is also included because the SRAM banks are loaded and read back through a test mode interface during simulation.

The twiddle ROM stores 512 complex twiddle factors. The ROM was initially modeled using a file initialized memory for RTL simulation. For synthesis and gate level simulation, it was replaced with a case based synthesizable ROM so that the twiddle constants were preserved in the synthesized netlist.

## IV. Butterfly Processing Element

Fig. 2 shows the butterfly PE architecture. The $B$ operand is first multiplied by the twiddle factor $W$. The multiplier result is then added to and subtracted from operand $A$ to form the two butterfly outputs. The final output stage applies one bit arithmetic scaling.

## V. Memory Architecture

The FFT processor uses a dual bank SRAM architecture, shown in Fig. 3. The two SRAM banks allow the controller to alternate the active read and write banks between FFT stages. In one stage, one bank supplies butterfly input data while the other receives updated butterfly outputs. In the next stage, the bank roles are exchanged. This ping pong memory organization avoids the need for a large multiport memory while still supporting in place style data reuse.

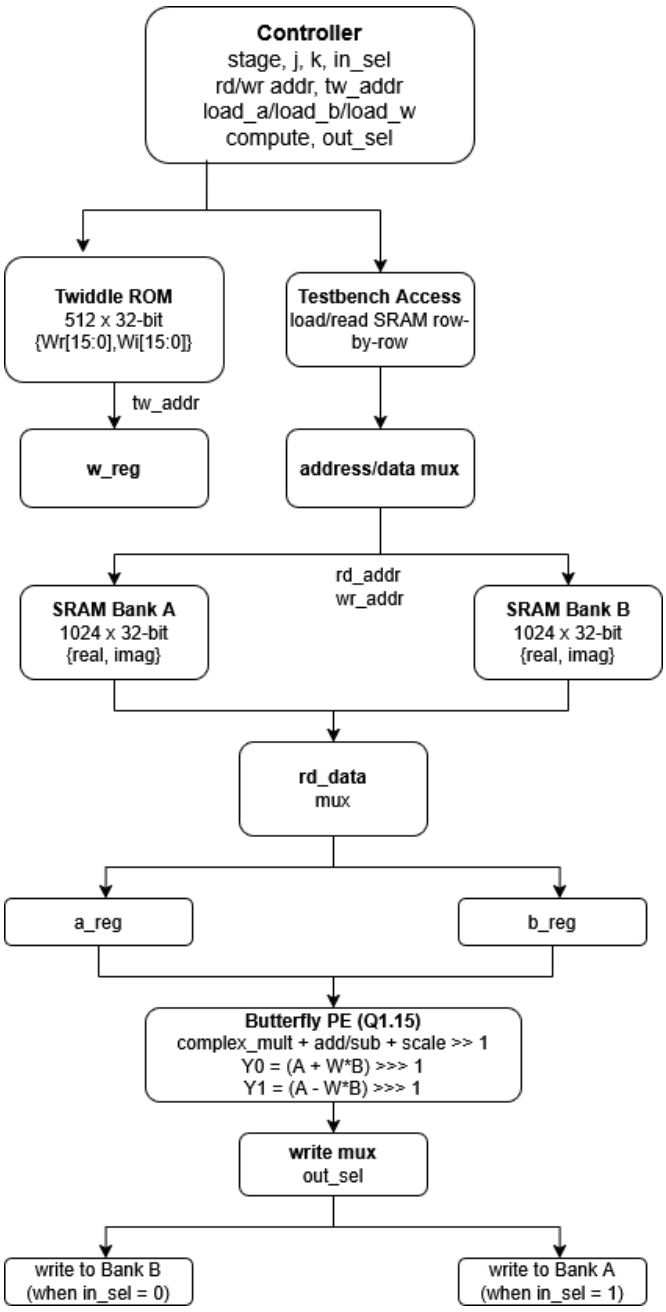



Fig. 1. Top level datapath block diagram of the FFT processor.

## VI. Controller ASM

Fig. 4 shows the controller ASM chart. The controller sequences SRAM reads, twiddle loading, butterfly computation, and writeback. Three nested loop indices are used: $j$ for butterfly position within a group, $k$ for group index, and $stage$ for the FFT stage. The twiddle address is generated as

$$\texttt{tw_addr} = j \ll (9 - stage). \tag{4}$$

The controller asserts `done` after all 10 FFT stages have completed.

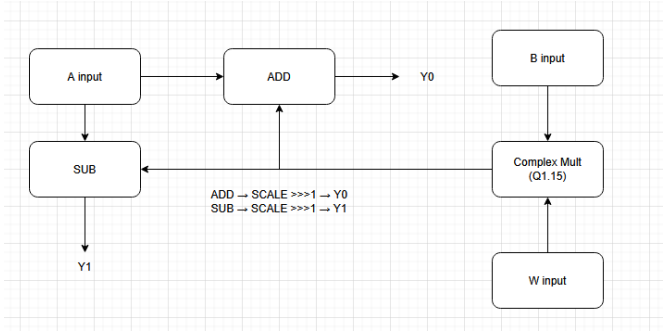



Fig. 2. Butterfly PE architecture using Q1.15 complex multiplication and per stage normalization.

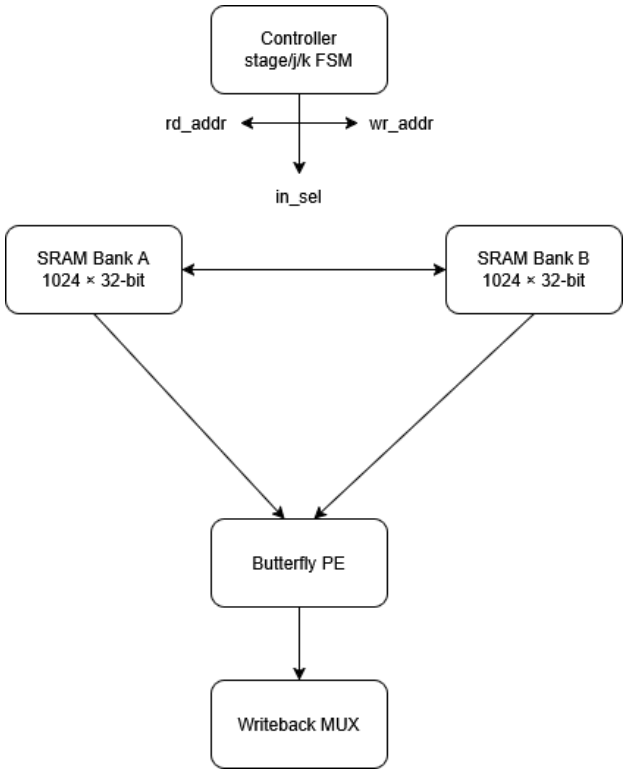



Fig. 3. Dual bank memory architecture used for ping pong read and write access across FFT stages.

## VII. Functional Verification

The design was verified using a SystemVerilog testbench. Input samples were loaded into the SRAM through a testbench access interface. After the FFT computation completed, the final SRAM contents were dumped to a text file and compared against a Python NumPy reference.

Fig. 5 shows the overall execution waveform. The processor starts when `start` is asserted, enters the busy state, iterates through FFT stages, and asserts `done` at the end of computation. Fig. 6 shows selected controller and address generation signals. Fig. 7 shows registered datapath operands and twiddle values during butterfly execution.

The waveform confirms that the controller correctly transi-

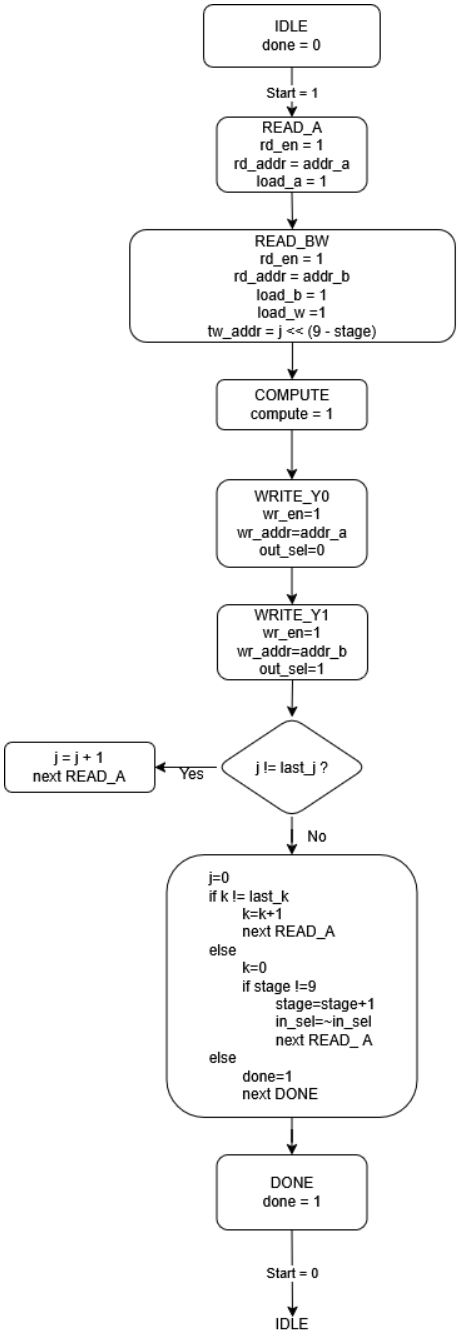



Fig. 4. ASM chart of the FFT controller.

tions from IDLE into active FFT execution after the start pulse. The busy signal remains asserted during all FFT stages and deasserts only after the final writeback operation completes. The done signal is asserted for one cycle after the completion of all 10 FFT stages.

The controller waveform verifies correct nested loop operation for the stage, j, and k indices. The generated SRAM addresses increment according to the butterfly access pattern, while the twiddle address follows the expected stage dependent shift relationship.

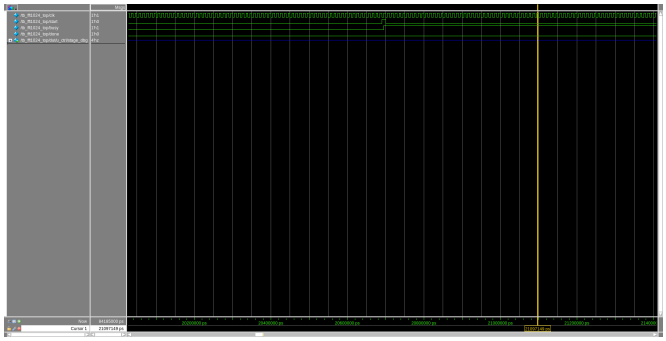


Fig. 5. Overall simulation waveform showing start, busy, done, and FFT stage progression.

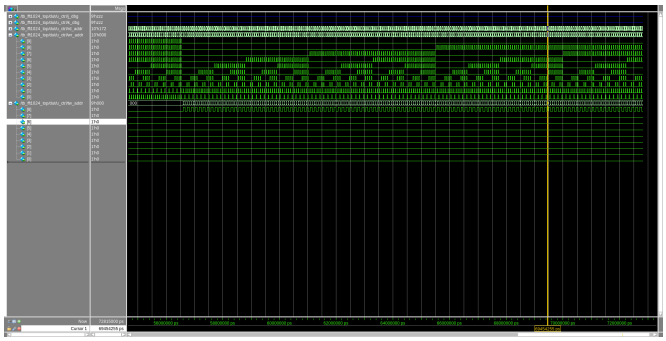


Fig. 6. Controller waveform showing loop counters and address generation.

The datapath waveform confirms that butterfly operands, twiddle factors, and output values are updated synchronously with the controller state progression. The registered values also verify that the Q1.15 arithmetic datapath produces bounded scaled outputs after each butterfly computation stage.

## VIII. Numerical Accuracy

The hardware FFT output was compared against a floating point Python reference scaled by $1/N$. The measured error was

$$\text{RMSE} = 3.7972 \times 10^{-5}, \tag{5}$$

with

$$\text{NRMSE}_{\text{rms}} = 1.1609 \times 10^{-2}. \tag{6}$$

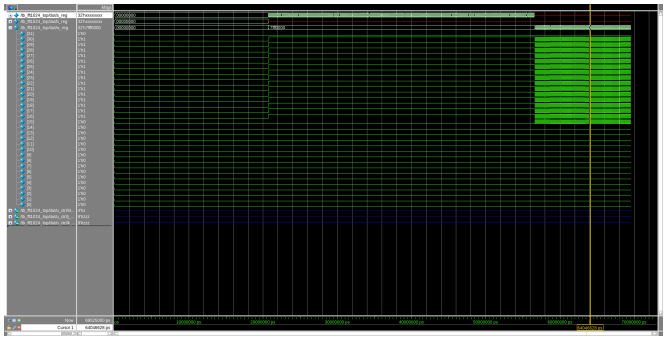


Fig. 7. Datapath waveform showing registered butterfly operands and twiddle values.

Selected output bins are listed in Table I. The close agreement confirms that the fixed point datapath, twiddle addressing, scaling, and memory ordering are consistent with the reference model.

TABLE I
SELECTED FFT OUTPUT BINS COMPARED WITH THE PYTHON REFERENCE.

| Bin | Hardware Output | Reference Output |
|---|---|---|
| 0 | $-0.005219 + j0.000000$ | $-0.005092 + j0.000000$ |
| 11 | $0.022888 + j0.001495$ | $0.022985 + j0.001537$ |
| 1013 | $0.022980 - j0.001556$ | $0.022985 - j0.001537$ |

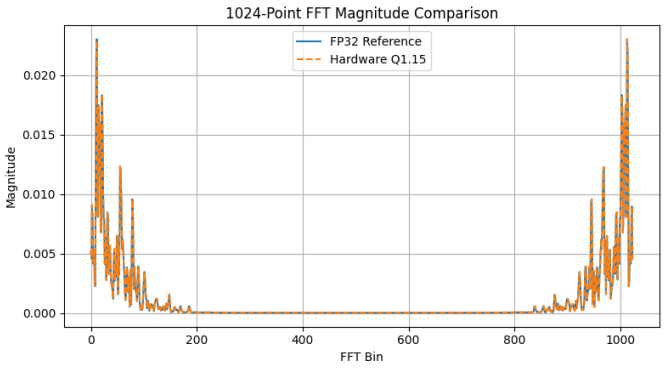



Fig. 8. Magnitude comparison between the FP32 reference FFT and the post-layout hardware FFT output.

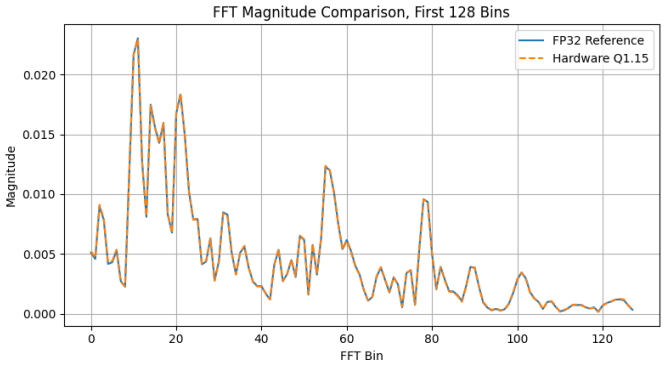



Fig. 9. Zoomed magnitude comparison for the first 128 FFT bins. The hardware result closely follows the FP32 reference.

## IX. SYNTHESIS AND SRAM MACRO INTEGRATION

The design was synthesized with Synopsys Design Compiler using the TSMC 65 nm standard cell library and DesignWare components. The memory subsystem was implemented using generated 1024 by 32 bit SRAM macros. The SRAM macro deliverables included Verilog simulation models, timing libraries, LEF view, GDS, CDL, and a Synopsys database library. The memory macro was preserved as a black box during synthesis and then integrated into the APR flow using its LEF and timing model.

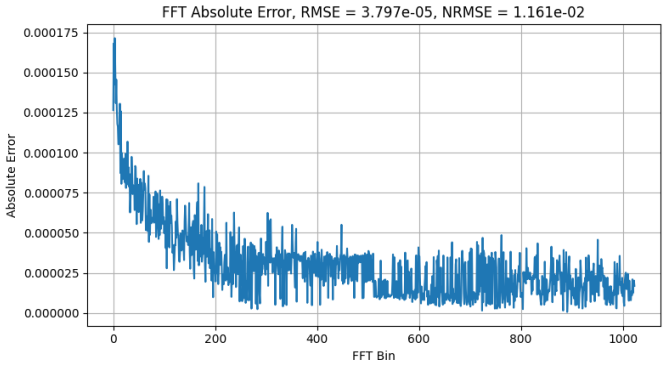



Fig. 10. Absolute FFT output error between the post-layout hardware result and the FP32 reference. The measured RMSE is $3.797 \times 10^{-5}$ and the RMS-normalized NRMSE is $1.161 \times 10^{-2}$.

Gate level simulation with the SRAM macro was performed after synthesis. The same FFT comparison flow was used, and the simulation produced the same numerical result as the RTL level verification, with RMSE $= 3.7972 \times 10^{-5}$ and NRMSE $= 1.1609 \times 10^{-2}$.

## X. PHYSICAL IMPLEMENTATION

The synthesized netlist was imported into Cadence Innovus. The APR flow included floorplanning, SRAM macro placement, power planning, standard cell placement, clock tree synthesis, routing, filler insertion, and extraction. The flow generated DEF, GDS, SPEF, SDF, and post route Verilog outputs.

Fig. 11 shows the floorplan. The layout area is dominated by the SRAM macros. The standard cell logic occupies the region to the right of the memory blocks. Fig. 12 shows the placement result, while Fig. 13 shows the post route layout.

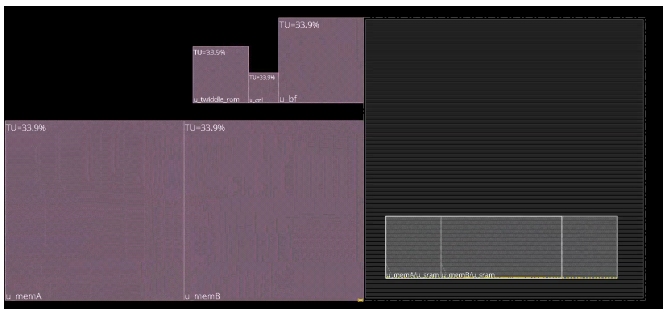


Fig. 11. FFT processor floorplan showing SRAM macros and the standard cell region.

## XI. POST LAYOUT TIMING AND POWER ANALYSIS

Post layout static timing analysis was performed using PrimeTime with the post route SPEF. A 10 ns clock period was used. The clocked setup path group reported a critical path length of 4.32 ns and a setup slack of 5.48 ns. The clocked hold path group reported a critical path length of 0.31 ns and a hold slack of 0.19 ns. No setup or hold violating paths were

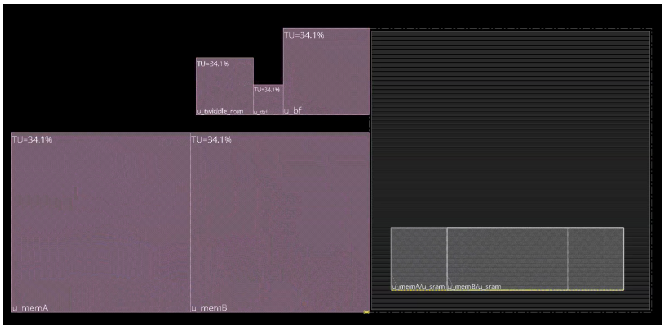


Fig. 12. Placement result after macro and standard cell placement.

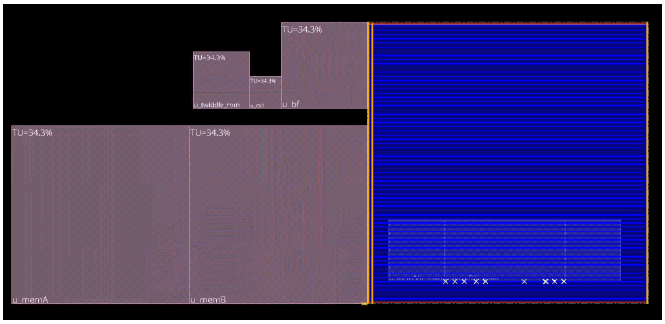


Fig. 13. Post route layout showing routed interconnect and SRAM macro integration.

```
Timing Path Group '**async_default**' (max_delay/setup)
-----------------------------------------
Levels of Logic:                         0
Critical Path Length:                 1.08
Critical Path Slack:                  8.84
Total Negative Slack:                 0.00
No. of Violating Paths:                  0
-----------------------------------------

Timing Path Group 'clk' (max_delay/setup)
-----------------------------------------
Levels of Logic:                        67
Critical Path Length:                 4.32
Critical Path Slack:                  5.48
Total Negative Slack:                 0.00
No. of Violating Paths:                  0
-----------------------------------------

Timing Path Group '**async_default**' (min_delay/hold)
-----------------------------------------
Levels of Logic:                         0
Critical Path Length:                 1.04
Critical Path Slack:                  0.85
Total Negative Slack:                 0.00
No. of Violating Paths:                  0
-----------------------------------------

Timing Path Group 'clk' (min_delay/hold)
-----------------------------------------
Levels of Logic:                         3
Critical Path Length:                 0.31
Critical Path Slack:                  0.19
Total Negative Slack:                 0.00
No. of Violating Paths:                  0
-----------------------------------------
```

Fig. 14. PrimeTime post layout timing summary.

reported in the clocked path group. The corresponding timing report screenshot is shown in Fig. 14.

The estimated maximum clock frequency was calculated from the post layout setup critical path:

$$f_{\max} \approx \frac{1}{4.32 \text{ ns}} = 231.5 \text{ MHz}. \tag{7}$$

The design was therefore verified at a conservative 100 MHz operating clock corresponding to the 10 ns project clock constraint.

The post-layout critical path is primarily associated with the butterfly processing element datapath. The path includes the complex multiplier, add/subtract logic, scaling operation, and routed interconnect delay between arithmetic stages. Since the FFT processor reuses a single butterfly PE across all FFT stages, this datapath dominates the overall timing behavior of the design.

The setup analysis corresponds to the maximum delay timing check, where data launched by one register must arrive at the destination register before the next active clock edge. The reported setup critical path length is 4.32 ns, which is significantly smaller than the applied 10 ns clock period constraint. As a result, the design achieves a positive setup slack of 5.48 ns and no setup timing violations are observed.

The hold analysis corresponds to the minimum delay timing check. In this case, the data must not propagate too quickly after the launching clock edge. The minimum delay critical path was measured as 0.31 ns, resulting in a positive hold slack of 0.19 ns. Therefore, the design also satisfies all hold timing requirements without additional hold fixing buffers.

The setup critical path mainly originates from the butterfly datapath, including complex multiplication, addition/subtraction logic, and the associated routing delay after placement and routing. Since the post-layout timing analysis includes extracted parasitic interconnect information from the SPEF file, the reported slack values reflect realistic routed timing behavior.

Power is reported from the available averaged power report. The estimated average power is 88.3 mW.

## XII. Performance Metrics

The project required six metrics: maximum clock frequency, throughput, energy efficiency, area, compute density, and accuracy. These metrics are summarized in Table III. The processor requires 27648 clock cycles for one 1024 point FFT transform including the control overhead used in the testbench evaluation.

At the conservative 100 MHz operating clock, the transform rate is

$$R_{\text{FFT}} = \frac{100 \times 10^6}{27648} = 3616.9 \text{ FFT/s}. \tag{8}$$

The sample throughput is therefore

$$T = 3616.9 \times 1024 = 3.70 \text{ MS/s}. \tag{9}$$

Using the estimated average power of 88.3 mW, the energy per FFT transform is

$$E_{\text{FFT}} = \frac{88.3 \times 10^{-3}}{3616.9} = 24.4 \ \mu\text{J/FFT}. \tag{10}$$

The corresponding energy per sample is

$$E_{\text{sample}} = \frac{88.3 \times 10^{-3}}{3.70 \times 10^{6}} = 23.9 \ \text{nJ/sample}. \tag{11}$$

The standard cell area is also reported because it reflects the synthesized logic area, while the full layout footprint includes SRAM macro area and routing resources. Since the SRAM macros dominate the physical design, the full layout footprint is the appropriate value for the final area and compute density metrics.

## XIII. Implementation Summary

Table II summarizes the main implementation results. The reported standard cell area is the logic cell area from PrimeTime QoR. The memory macro area is visible in the physical layout and dominates the full block footprint.

TABLE II
IMPLEMENTATION SUMMARY.

| Metric | Value |
|---|---|
| FFT size | 1024 points |
| Algorithm | Radix 2 DIT |
| Fixed point format | Q1.15 |
| Number of stages | 10 |
| Clock constraint | 10 ns |
| Setup critical path | 4.32 ns |
| Setup slack | 5.48 ns |
| Hold critical path | 0.31 ns |
| Hold slack | 0.19 ns |
| Total negative slack | 0.00 ns |
| Violating timing paths | 0 |
| Leaf cell count | 4820 |
| Standard cell area | 85836.44 $\mu$m$^2$ |
| Estimated averaged power | 88.3 mW |
| RMSE | $3.7972 \times 10^{-5}$ |
| $\text{NRMSE}_{\text{rms}}$ | $1.1609 \times 10^{-2}$ |

TABLE III
FINAL FFT PROCESSOR METRICS.

| Metric | Value |
|---|---|
| Maximum clock frequency | 231.5 MHz |
| Throughput | 3.70 MS/s |
| Energy efficiency | 23.9 nJ/sample |
| Area | 0.250 mm$^2$ |
| Compute density | 14.8 MS/s/mm$^2$ |
| Accuracy | $\text{NRMSE}_{\text{rms}} = 1.1609 \times 10^{-2}$ |

## XIV. Layout Verification Status

The Innovus APR flow generated routed GDS, DEF, SPEF, SDF, and post route Verilog files. The generated layout was inspected at the APR level, and post layout PrimeTime analysis confirmed clean setup and hold timing under the target clock constraint.

## XV. Discussion

The implementation demonstrates that a single butterfly PE with dual SRAM banks can implement a 1024 point FFT with moderate standard cell area. The use of per stage scaling simplifies overflow control and provides a direct match to the $1/N$ scaled reference FFT. The primary physical design characteristic is that the memory macros dominate the layout footprint, while the arithmetic and controller logic occupy a smaller standard cell region.

The large positive setup slack indicates that the design is not frequency limited under the current 100 MHz operating target. The implemented radix-2 architecture therefore trades throughput efficiency for reduced hardware complexity by reusing a single butterfly PE instead of employing a fully parallel FFT structure. This substantially reduces arithmetic area at the expense of longer transform latency.

Several implementation issues were identified and resolved during the backend flow. The twiddle ROM had to be converted from a file initialized behavioral memory into a synthesizable ROM so that the constants were preserved in the gate level netlist. The SRAM macro model also required a synchronous access compatible testbench so that read and write timing matched the macro behavior. After these fixes, both gate level and post APR functional simulation matched the Python reference.

Although full industrial signoff verification was beyond the available project schedule, the implemented APR flow successfully generated routed GDS, SPEF, SDF, and post layout timing models without major timing issues. The final PrimeTime results showed no setup or hold violations at the 10 ns clock constraint.

## XVI. Conclusion

A 1024 point fixed point FFT processor was designed, verified, synthesized, and physically implemented. The design uses a radix 2 architecture, Q1.15 fixed point arithmetic, a reusable butterfly PE, a synthesizable twiddle ROM, and a dual SRAM bank memory subsystem. Functional simulation, gate level simulation, and post APR simulation all matched the Python reference with RMSE $= 3.7972 \times 10^{-5}$. The physical implementation generated GDS, DEF, SPEF, SDF, and post route netlist files. Post layout timing analysis at a 10 ns clock period showed 5.48 ns setup slack and 0.19 ns hold slack, demonstrating that the design satisfies the timing target. The six project metrics were also extracted, including maximum frequency, throughput, energy efficiency, area, compute density, and numerical accuracy.

Supplementary implementation files:

https://drive.google.com/file/d/1NcuRdzCLm0_0u-JpQNgvF8eOpA-LuLHr/view?usp=sharing

```
1   `timescale 1ns/1ps
2   module fft1024_top #(
3       parameter int N = 1024,
4       parameter int LOGN = 10,
5       parameter int TW_N = 512
6   )(
7       input  logic        clk,
8       input  logic        rst_n,
9       input  logic        start,
10
11      output logic        done,
12      output logic        busy,
13
14      input  logic        tb_mode,
15      input  logic        tb_we,
16      input  logic        tb_bank_sel,
17      input  logic [9:0]  tb_addr,
18      input  logic [31:0] tb_wdata,
19      output logic [31:0] tb_rdata
20  );
21
22      logic [31:0] memA_dout, memB_dout;
23      logic        memA_cs, memA_we;
24      logic [9:0]  memA_addr;
25      logic [31:0] memA_din;
26
27      logic        memB_cs, memB_we;
28      logic [9:0]  memB_addr;
29      logic [31:0] memB_din;
30
31      logic [31:0] tw_data;
32
33      logic        in_sel;
34      logic        rd_en;
35      logic [9:0]  rd_addr;
36      logic        wr_en;
37      logic [9:0]  wr_addr;
38      logic [8:0]  tw_addr;
39      logic        load_a;
40      logic        load_b;
41      logic        load_w;
42      logic        compute;
43      logic        out_sel;
44
45      logic [3:0] stage_dbg;
46      logic [3:0] state_dbg;
47      logic [8:0]  j_dbg;
48      logic [8:0]  k_dbg;
49
50      logic [31:0] rd_data;
51      logic [31:0] a_reg;
52      logic [31:0] b_reg;
53      logic [31:0] w_reg;
54      logic [31:0] y0;
55      logic [31:0] y1;
56      logic [31:0] wr_data;
57
58      twiddle_rom_q15 u_twiddle_rom (
59          .addr(tw_addr),
60          .data(tw_data)
61      );
62
63
64      fft1024_controller u_ctrl (
65          .clk       (clk),
66          .rst_n     (rst_n),
67          .start     (start),
68          .done      (done),
69          .busy      (busy),
70          .in_sel    (in_sel),
71          .rd_en     (rd_en),
72          .rd_addr   (rd_addr),
73          .wr_en     (wr_en),
74          .wr_addr   (wr_addr),
75          .tw_addr   (tw_addr),
76          .load_a    (load_a),
```

```
77              .load_b    (load_b),
78              .load_w    (load_w),
79              .compute   (compute),
80              .out_sel   (out_sel),
81              .stage_dbg (stage_dbg),
82              .j_dbg     (j_dbg),
83              .k_dbg     (k_dbg),
84              .state_dbg (state_dbg)
85          );
86
87          butterfly_pe_q15 u_bf (
88              .A  (a_reg),
89              .B  (b_reg),
90              .W  (w_reg),
91              .Y0 (y0),
92              .Y1 (y1)
93          );
94
95          sram_wrapper u_memA (
96              .clk  (clk),
97              .cs   (memA_cs),
98              .we   (memA_we),
99              .addr (memA_addr),
100             .din  (memA_din),
101             .dout (memA_dout)
102         );
103
104         sram_wrapper u_memB (
105             .clk  (clk),
106             .cs   (memB_cs),
107             .we   (memB_we),
108             .addr (memB_addr),
109             .din  (memB_din),
110             .dout (memB_dout)
111         );
112
113         assign wr_data = (out_sel == 1'b0) ? y0 : y1;
114
115         always_comb begin
116             memA_cs   = 1'b1;
117             memB_cs   = 1'b1;
118             memA_we   = 1'b0;
119             memB_we   = 1'b0;
120             memA_addr = 10'd0;
121             memB_addr = 10'd0;
122             memA_din  = 32'd0;
123             memB_din  = 32'd0;
124             tb_rdata  = 32'd0;
125             rd_data   = 32'd0;
126
127             if (tb_mode) begin
128                 if (tb_bank_sel == 1'b0) begin
129                     memA_addr = tb_addr;
130                     memA_we   = tb_we;
131                     memA_din  = tb_wdata;
132                     tb_rdata  = memA_dout;
133                 end else begin
134                     memB_addr = tb_addr;
135                     memB_we   = tb_we;
136                     memB_din  = tb_wdata;
137                     tb_rdata  = memB_dout;
138                 end
139             end else begin
140                 if (in_sel == 1'b0) begin
141                     // read A, write B
142                     memA_addr = rd_addr;
143                     rd_data   = memA_dout;
144
145                     memB_addr = wr_addr;
146                     memB_we   = wr_en;
147                     memB_din  = wr_data;
148                 end else begin
149                     // read B, write A
150                     memB_addr = rd_addr;
151                     rd_data   = memB_dout;
152
```

```
153                     memA_addr  = wr_addr;
154                     memA_we    = wr_en;
155                     memA_din   = wr_data;
156                 end
157             end
158         end
159
160         always_ff @(posedge clk or negedge rst_n) begin
161             if (!rst_n) begin
162                 a_reg <= 32'd0;
163                 b_reg <= 32'd0;
164                 w_reg <= 32'd0;
165             end else if (!tb_mode) begin
166                 if (load_a)
167                     a_reg <= rd_data;
168                 if (load_b)
169                     b_reg <= rd_data;
170                 if (load_w)
171                     w_reg <= tw_data;
172             end
173         end
174
175     endmodule
176
```

```
1   `timescale 1ns/1ps
2
3   module fft1024_controller (
4       input  logic        clk,
5       input  logic        rst_n,
6       input  logic        start,
7
8       output logic        done,
9       output logic        busy,
10
11      // select source/destination memory bank
12      // 0: read A write B
13      // 1: read B write A
14      output logic        in_sel,
15
16      // read-side control
17      output logic        rd_en,
18      output logic [9:0]  rd_addr,
19
20      // write-side control
21      output logic        wr_en,
22      output logic [9:0]  wr_addr,
23
24      // twiddle ROM
25      output logic [8:0]  tw_addr,
26
27      // local control for datapath
28      output logic        load_a,
29      output logic        load_b,
30      output logic        load_w,
31      output logic        compute,
32      // 0 -> write Y0, 1 -> write Y1
33      output logic        out_sel,
34
35      // optional observability/debug
36      output logic [3:0]  stage_dbg,
37      output logic [8:0]  j_dbg,
38      output logic [8:0]  k_dbg,
39      output logic [3:0] state_dbg
40  );
41
42      localparam int N      = 1024;
43      localparam int LOGN   = 10;
44      localparam int STAGES = 10;
45
46     typedef enum logic [3:0] {
47         S_IDLE     = 4'd0,
48         S_SET_A    = 4'd1,
49         S_LOAD_A   = 4'd2,
50         S_SET_BW   = 4'd3,
51         S_LOAD_BW  = 4'd4,
52         S_COMPUTE  = 4'd5,
53         S_WRITE_Y0 = 4'd6,
54         S_WRITE_Y1 = 4'd7,
55         S_DONE     = 4'd8
56     } state_t;
57
58      state_t state, state_n;
59
60      logic [3:0] stage, stage_n;   // 0..9
61      logic [8:0] j, j_n;           // 0..half_m-1
62      logic [8:0] k, k_n;           // 0..N/m-1
63      logic       in_sel_n;
64      logic       done_n;
65
66      logic [9:0] half_m;
67      logic [9:0] m;
68      logic [9:0] addr_a;
69      logic [9:0] addr_b;
70      logic [8:0] last_j;
71      logic [8:0] last_k;
72
73      // Combinational address formulas
74      assign half_m = 10'd1 << stage;
75      assign m = half_m << 1;
76      assign addr_a = k * m + j;
```

```
77        assign addr_b = addr_a + half_m;
78
79        // twiddle_index = j << (9 - stage)
80        assign tw_addr = j << (LOGN - 1 - stage);
81
82        assign last_j = half_m - 1'b1;
83        assign last_k = (9'd1 << (LOGN - stage - 1)) - 1'b1;
84
85        assign stage_dbg = stage;
86        assign j_dbg     = j;
87        assign k_dbg     = k;
88        assign state_dbg = state;
89
90        always_ff @(posedge clk or negedge rst_n) begin
91            if (!rst_n) begin
92                state  <= S_IDLE;
93                stage  <= 4'd0;
94                j      <= 9'd0;
95                k      <= 9'd0;
96                in_sel <= 1'b0;
97                done   <= 1'b0;
98            end else begin
99                state  <= state_n;
100               stage  <= stage_n;
101               j      <= j_n;
102               k      <= k_n;
103               in_sel <= in_sel_n;
104               done   <= done_n;
105           end
106       end
107
108       // Default next-state / outputs
109       always_comb begin
110           state_n  = state;
111           stage_n  = stage;
112           j_n      = j;
113           k_n      = k;
114           in_sel_n = in_sel;
115           done_n   = done;
116
117           busy     = (state != S_IDLE) && (state != S_DONE);
118
119           rd_en    = 1'b0;
120           rd_addr  = 10'd0;
121           wr_en    = 1'b0;
122           wr_addr  = 10'd0;
123
124           load_a   = 1'b0;
125           load_b   = 1'b0;
126           load_w   = 1'b0;
127           compute  = 1'b0;
128           out_sel  = 1'b0;
129
130           case (state)
131               S_IDLE: begin
132             done_n = 1'b0;
133             if (start) begin
134              stage_n  = 4'd0;
135              j_n      = 9'd0;
136              k_n      = 9'd0;
137              in_sel_n = 1'b0;
138              state_n  = S_SET_A;
139               end
140         end
141
142         S_SET_A: begin
143             rd_en    = 1'b1;
144             rd_addr = addr_a;
145             state_n = S_LOAD_A;
146         end
147
148         S_LOAD_A: begin
149             rd_en    = 1'b1;
150             rd_addr = addr_a;
151             load_a   = 1'b1;
152             state_n = S_SET_BW;
```

```
153          end
154
155          S_SET_BW: begin
156              rd_en   = 1'b1;
157              rd_addr = addr_b;
158              state_n = S_LOAD_BW;
159          end
160
161          S_LOAD_BW: begin
162              rd_en   = 1'b1;
163              rd_addr = addr_b;
164              load_b  = 1'b1;
165              load_w  = 1'b1;
166              state_n = S_COMPUTE;
167          end
168
169          S_COMPUTE: begin
170              compute = 1'b1;
171              state_n = S_WRITE_Y0;
172          end
173
174          S_WRITE_Y0: begin
175              wr_en   = 1'b1;
176              wr_addr = addr_a;
177              out_sel = 1'b0;
178              state_n = S_WRITE_Y1;
179          end
180
181          S_WRITE_Y1: begin
182              wr_en   = 1'b1;
183              wr_addr = addr_b;
184              out_sel = 1'b1;
185
186              if (j != last_j) begin
187             j_n     = j + 1'b1;
188             state_n = S_SET_A;
189              end else begin
190             j_n = 9'd0;
191             if (k != last_k) begin
192                 k_n     = k + 1'b1;
193                 state_n = S_SET_A;
194             end else begin
195                 k_n = 9'd0;
196                 if (stage != STAGES-1) begin
197                stage_n  = stage + 1'b1;
198                in_sel_n = ~in_sel;
199                state_n  = S_SET_A;
200                 end else begin
201                done_n  = 1'b1;
202                state_n = S_DONE;
203                 end
204             end
205              end
206          end
207
208          S_DONE: begin
209              if (!start) begin
210             state_n = S_IDLE;
211              end
212          end
213
214                default: begin
215                    state_n = S_IDLE;
216                end
217            endcase
218        end
219
220    endmodule
221
```

```
1   `timescale 1ns/1ps
2
3   module complex_mult_q15 (
4       input  logic signed [15:0] ar,
5       input  logic signed [15:0] ai,
6       input  logic signed [15:0] br,
7       input  logic signed [15:0] bi,
8       output logic signed [15:0] pr,
9       output logic signed [15:0] pi
10  );
11
12      logic signed [31:0] arbr, aibi, arbi, aibr;
13      logic signed [32:0] real_tmp, imag_tmp;
14
15      always_comb begin
16          arbr = ar * br;
17          aibi = ai * bi;
18          arbi = ar * bi;
19          aibr = ai * br;
20
21          real_tmp = arbr - aibi;   // Q2.30
22          imag_tmp = arbi + aibr;   // Q2.30
23
24          pr = real_tmp >>> 15;     // back to Q1.15
25          pi = imag_tmp >>> 15;
26      end
27
28  endmodule
29
```

```
`timescale 1ns/1ps

module butterfly_pe_q15 (
    input  logic [31:0] A,
    input  logic [31:0] B,
    input  logic [31:0] W,
    output logic [31:0] Y0,
    output logic [31:0] Y1
);

    logic signed [15:0] Ar, Ai;
    logic signed [15:0] Br, Bi;
    logic signed [15:0] Wr, Wi;

    logic signed [15:0] Tr, Ti;
    logic signed [16:0] Y0r_tmp, Y0i_tmp, Y1r_tmp, Y1i_tmp;
    logic signed [16:0] Y0r_scl, Y0i_scl, Y1r_scl, Y1i_scl;
    logic signed [15:0] Y0r, Y0i, Y1r, Y1i;

    assign Ar = A[31:16];
    assign Ai = A[15:0];
    assign Br = B[31:16];
    assign Bi = B[15:0];
    assign Wr = W[31:16];
    assign Wi = W[15:0];

    complex_mult_q15 u_mult (
        .ar(Wr),
        .ai(Wi),
        .br(Br),
        .bi(Bi),
        .pr(Tr),
        .pi(Ti)
    );

    always_comb begin
        // butterfly add/sub
        Y0r_tmp = Ar + Tr;
        Y0i_tmp = Ai + Ti;
        Y1r_tmp = Ar - Tr;
        Y1i_tmp = Ai - Ti;

        // stage scaling: divide by 2 every stage
        Y0r_scl = Y0r_tmp >>> 1;
        Y0i_scl = Y0i_tmp >>> 1;
        Y1r_scl = Y1r_tmp >>> 1;
        Y1i_scl = Y1i_tmp >>> 1;

        // simple truncate back to 16-bit
        Y0r = Y0r_scl[15:0];
        Y0i = Y0i_scl[15:0];
        Y1r = Y1r_scl[15:0];
        Y1i = Y1i_scl[15:0];
    end

    assign Y0 = {Y0r, Y0i};
    assign Y1 = {Y1r, Y1i};

endmodule

```

```
`timescale 1ns/1ps

module sram_wrapper #(
    parameter int DEPTH = 1024,
    parameter int AW = 10
)(
    input  logic          clk,
    input  logic          cs,
    input  logic          we,
    input  logic [AW-1:0] addr,
    input  logic [31:0]   din,
    output logic [31:0]   dout
);

    logic        cen_n;
    logic        gwen_n;
    logic [3:0]  wen_n;

    assign cen_n  = ~cs;
    assign gwen_n = ~we;
    assign wen_n  = we ? 4'b0000 : 4'b1111;

    sram1024x32 u_sram (
        .Q    (dout),
        .CLK  (clk),
        .CEN  (cen_n),
        .WEN  (wen_n),
        .A    (addr),
        .D    (din),
        .EMA  (3'b000),
        .GWEN (gwen_n),
        .RETN (1'b1)
    );

endmodule

```

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 10
Design : fft1024_top
Version: U-2022.12-SP7
Date   : Mon May 11 23:27:30 2026
****************************************

Operating Conditions: NCCOM   Library: tcbn65gplustc_ccs
Wire Load Model Mode: segmented

  Startpoint: w_reg_reg[17]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: u_memA/u_sram
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  sram_wrapper_0     ZeroWireload          tcbn65gplustc_ccs
  sram_wrapper_1     ZeroWireload          tcbn65gplustc_ccs
  fft1024_top        ZeroWireload          tcbn65gplustc_ccs
  fft1024_controller ZeroWireload          tcbn65gplustc_ccs
  complex_mult_q15   ZeroWireload          tcbn65gplustc_ccs
  butterfly_pe_q15   ZeroWireload          tcbn65gplustc_ccs

  Point                                                   Incr       Path
  ---------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  w_reg_reg[17]/CP (DFCNQD1)                              0.00       0.00 r
  w_reg_reg[17]/Q (DFCNQD1)                               0.09       0.09 r
  u_bf/W[17] (butterfly_pe_q15)                           0.00       0.09 r
  u_bf/u_mult/ar[1] (complex_mult_q15)                    0.00       0.09 r
  u_bf/u_mult/U211/ZN (INVD0)                             0.04       0.13 f
  u_bf/u_mult/U216/ZN (AOI22D0)                           0.12       0.25 r
  u_bf/u_mult/U292/ZN (INVD0)                             0.05       0.30 f
  u_bf/u_mult/U294/Z (OR2D0)                              0.06       0.36 f
  u_bf/u_mult/U295/ZN (INVD0)                             0.13       0.49 r
  u_bf/u_mult/U1197/ZN (AOI22D0)                          0.05       0.55 f
  u_bf/u_mult/U1198/ZN (OAI221D0)                         0.05       0.60 r
  u_bf/u_mult/DP_OP_7J2_125_8831/U272/S (CMPE42D1)        0.17       0.77 f
  u_bf/u_mult/U838/ZN (MAOI222D0)                         0.06       0.82 r
  u_bf/u_mult/U839/ZN (INVD0)                             0.02       0.84 f
  u_bf/u_mult/U840/ZN (MAOI222D0)                         0.06       0.90 r
  u_bf/u_mult/U841/ZN (INVD0)                             0.02       0.93 f
```

```
u_bf/u_mult/U842/ZN (MAOI222D0)                    0.06       0.98 r
u_bf/u_mult/U843/ZN (INVD0)                        0.02       1.00 f
u_bf/u_mult/U844/ZN (MAOI222D0)                    0.06       1.06 r
u_bf/u_mult/U845/ZN (INVD0)                        0.02       1.09 f
u_bf/u_mult/U846/ZN (MAOI222D0)                    0.06       1.14 r
u_bf/u_mult/U847/ZN (INVD0)                        0.02       1.16 f
u_bf/u_mult/U848/ZN (MAOI222D0)                    0.06       1.22 r
u_bf/u_mult/U849/ZN (INVD0)                        0.02       1.24 f
u_bf/u_mult/U850/ZN (MAOI222D0)                    0.06       1.30 r
u_bf/u_mult/U851/ZN (INVD0)                        0.02       1.32 f
u_bf/u_mult/U852/ZN (MAOI222D0)                    0.06       1.38 r
u_bf/u_mult/U853/ZN (INVD0)                        0.02       1.40 f
u_bf/u_mult/U854/ZN (MAOI222D0)                    0.06       1.46 r
u_bf/u_mult/U855/ZN (INVD0)                        0.02       1.48 f
u_bf/u_mult/U856/ZN (MAOI222D0)                    0.06       1.54 r
u_bf/u_mult/U857/ZN (INVD0)                        0.02       1.56 f
u_bf/u_mult/U858/ZN (MAOI222D0)                    0.06       1.62 r
u_bf/u_mult/U859/ZN (INVD0)                        0.02       1.64 f
u_bf/u_mult/U860/ZN (MAOI222D0)                    0.06       1.70 r
u_bf/u_mult/U861/ZN (INVD0)                        0.02       1.72 f
u_bf/u_mult/intadd_2/U16/CO (FA1D0)                0.06       1.78 f
u_bf/u_mult/intadd_2/U15/S (FA1D0)                 0.07       1.85 f
u_bf/u_mult/pr[1] (complex_mult_q15)               0.00       1.85 f
u_bf/U47/ZN (MAOI222D0)                            0.07       1.92 r
u_bf/U48/ZN (INVD0)                                0.03       1.96 f
u_bf/U49/ZN (MAOI222D0)                            0.07       2.03 r
u_bf/U50/ZN (INVD0)                                0.03       2.05 f
u_bf/U51/ZN (MAOI222D0)                            0.07       2.13 r
u_bf/U52/ZN (INVD0)                                0.03       2.16 f
u_bf/U53/ZN (MAOI222D0)                            0.07       2.23 r
u_bf/U54/ZN (INVD0)                                0.03       2.26 f
u_bf/U55/ZN (MAOI222D0)                            0.07       2.34 r
u_bf/U56/ZN (INVD0)                                0.03       2.37 f
u_bf/U57/ZN (MAOI222D0)                            0.07       2.44 r
u_bf/U58/ZN (INVD0)                                0.03       2.47 f
u_bf/U59/ZN (MAOI222D0)                            0.07       2.54 r
u_bf/U60/ZN (INVD0)                                0.03       2.57 f
u_bf/U61/ZN (MAOI222D0)                            0.07       2.64 r
u_bf/U62/ZN (INVD0)                                0.03       2.67 f
u_bf/U63/ZN (MAOI222D0)                            0.07       2.75 r
u_bf/U64/ZN (INVD0)                                0.03       2.78 f
u_bf/U65/ZN (MAOI222D0)                            0.07       2.85 r
u_bf/U66/ZN (INVD0)                                0.03       2.88 f
u_bf/U67/ZN (MAOI222D0)                            0.07       2.95 r
u_bf/U68/ZN (INVD0)                                0.03       2.98 f
u_bf/U69/ZN (MAOI222D0)                            0.07       3.05 r
u_bf/U70/ZN (INVD0)                                0.03       3.08 f
u_bf/U71/ZN (MAOI222D0)                            0.07       3.16 r
u_bf/U72/ZN (INVD0)                                0.03       3.19 f
u_bf/U73/ZN (MAOI222D0)                            0.07       3.26 r
```

```
u_bf/U74/ZN (INVD0)                                      0.03       3.29 f
u_bf/U75/ZN (MAOI222D0)                                  0.08       3.37 r
u_bf/Y0[31] (butterfly_pe_q15)                           0.00       3.37 r
U436/Z (AO222D0)                                         0.07       3.44 r
u_memA/din[31] (sram_wrapper_1)                          0.00       3.44 r
u_memA/u_sram/D[31] (sram1024x32)                        0.00       3.44 r
data arrival time                                                   3.44

clock clk (rise edge)                                   10.00      10.00
clock network delay (ideal)                              0.00      10.00
clock uncertainty                                       -0.10       9.90
u_memA/u_sram/CLK (sram1024x32)                          0.00       9.90 r
library setup time                                      -0.09       9.81
data required time                                                  9.81
--------------------------------------------------------------------------
data required time                                                  9.81
data arrival time                                                  -3.44
--------------------------------------------------------------------------
slack (MET)                                                         6.37


Startpoint: w_reg_reg[17]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: u_memA/u_sram
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
sram_wrapper_0     ZeroWireload          tcbn65gplustc_ccs
sram_wrapper_1     ZeroWireload          tcbn65gplustc_ccs
fft1024_top        ZeroWireload          tcbn65gplustc_ccs
fft1024_controller ZeroWireload          tcbn65gplustc_ccs
complex_mult_q15   ZeroWireload          tcbn65gplustc_ccs
butterfly_pe_q15   ZeroWireload          tcbn65gplustc_ccs

Point                                                    Incr       Path
--------------------------------------------------------------------------
clock clk (rise edge)                                    0.00       0.00
clock network delay (ideal)                              0.00       0.00
w_reg_reg[17]/CP (DFCNQD1)                               0.00       0.00 r
w_reg_reg[17]/Q (DFCNQD1)                                0.09       0.09 r
u_bf/W[17] (butterfly_pe_q15)                            0.00       0.09 r
u_bf/u_mult/ar[1] (complex_mult_q15)                     0.00       0.09 r
u_bf/u_mult/U211/ZN (INVD0)                              0.04       0.13 f
u_bf/u_mult/U216/ZN (AOI22D0)                            0.12       0.25 r
u_bf/u_mult/U292/ZN (INVD0)                              0.05       0.30 f
u_bf/u_mult/U294/Z (OR2D0)                               0.06       0.36 f
u_bf/u_mult/U295/ZN (INVD0)                              0.13       0.49 r
```

```
u_bf/u_mult/U1487/ZN (AOI22D0)                          0.05       0.55 f
u_bf/u_mult/U1488/ZN (OAI221D0)                         0.05       0.60 r
u_bf/u_mult/DP_OP_8J2_126_8831/U272/S (CMPE42D1)        0.17       0.77 f
u_bf/u_mult/U887/ZN (MAOI222D0)                         0.06       0.82 r
u_bf/u_mult/U888/ZN (INVD0)                             0.02       0.84 f
u_bf/u_mult/U889/ZN (MAOI222D0)                         0.06       0.90 r
u_bf/u_mult/U890/ZN (INVD0)                             0.02       0.93 f
u_bf/u_mult/U891/ZN (MAOI222D0)                         0.06       0.98 r
u_bf/u_mult/U892/ZN (INVD0)                             0.02       1.00 f
u_bf/u_mult/U893/ZN (MAOI222D0)                         0.06       1.06 r
u_bf/u_mult/U894/ZN (INVD0)                             0.02       1.09 f
u_bf/u_mult/U895/ZN (MAOI222D0)                         0.06       1.14 r
u_bf/u_mult/U896/ZN (INVD0)                             0.02       1.16 f
u_bf/u_mult/U897/ZN (MAOI222D0)                         0.06       1.22 r
u_bf/u_mult/U898/ZN (INVD0)                             0.02       1.24 f
u_bf/u_mult/U899/ZN (MAOI222D0)                         0.06       1.30 r
u_bf/u_mult/U900/ZN (INVD0)                             0.02       1.32 f
u_bf/u_mult/U901/ZN (MAOI222D0)                         0.06       1.38 r
u_bf/u_mult/U902/ZN (INVD0)                             0.02       1.40 f
u_bf/u_mult/U903/ZN (MAOI222D0)                         0.06       1.46 r
u_bf/u_mult/U904/ZN (INVD0)                             0.02       1.48 f
u_bf/u_mult/U905/ZN (MAOI222D0)                         0.06       1.54 r
u_bf/u_mult/U906/ZN (INVD0)                             0.02       1.56 f
u_bf/u_mult/U907/ZN (MAOI222D0)                         0.06       1.62 r
u_bf/u_mult/U908/ZN (INVD0)                             0.02       1.64 f
u_bf/u_mult/U909/ZN (MAOI222D0)                         0.06       1.70 r
u_bf/u_mult/U910/ZN (INVD0)                             0.02       1.72 f
u_bf/u_mult/intadd_1/U16/CO (FA1D0)                     0.06       1.78 f
u_bf/u_mult/intadd_1/U15/S (FA1D0)                      0.07       1.85 f
u_bf/u_mult/pi[1] (complex_mult_q15)                    0.00       1.85 f
u_bf/U122/ZN (MAOI222D0)                                0.07       1.92 r
u_bf/U123/ZN (INVD0)                                    0.03       1.96 f
u_bf/U124/ZN (MAOI222D0)                                0.07       2.03 r
u_bf/U125/ZN (INVD0)                                    0.03       2.05 f
u_bf/U126/ZN (MAOI222D0)                                0.07       2.13 r
u_bf/U127/ZN (INVD0)                                    0.03       2.16 f
u_bf/U128/ZN (MAOI222D0)                                0.07       2.23 r
u_bf/U129/ZN (INVD0)                                    0.03       2.26 f
u_bf/U130/ZN (MAOI222D0)                                0.07       2.34 r
u_bf/U131/ZN (INVD0)                                    0.03       2.37 f
u_bf/U132/ZN (MAOI222D0)                                0.07       2.44 r
u_bf/U133/ZN (INVD0)                                    0.03       2.47 f
u_bf/U134/ZN (MAOI222D0)                                0.07       2.54 r
u_bf/U135/ZN (INVD0)                                    0.03       2.57 f
u_bf/U136/ZN (MAOI222D0)                                0.07       2.64 r
u_bf/U137/ZN (INVD0)                                    0.03       2.67 f
u_bf/U138/ZN (MAOI222D0)                                0.07       2.75 r
u_bf/U139/ZN (INVD0)                                    0.03       2.78 f
u_bf/U140/ZN (MAOI222D0)                                0.07       2.85 r
u_bf/U141/ZN (INVD0)                                    0.03       2.88 f
```

```
u_bf/U142/ZN (MAOI222D0)                                 0.07       2.95 r
u_bf/U143/ZN (INVD0)                                     0.03       2.98 f
u_bf/U144/ZN (MAOI222D0)                                 0.07       3.05 r
u_bf/U145/ZN (INVD0)                                     0.03       3.08 f
u_bf/U146/ZN (MAOI222D0)                                 0.07       3.16 r
u_bf/U147/ZN (INVD0)                                     0.03       3.19 f
u_bf/U148/ZN (MAOI222D0)                                 0.07       3.26 r
u_bf/U149/ZN (INVD0)                                     0.03       3.29 f
u_bf/U150/ZN (MAOI222D0)                                 0.08       3.37 r
u_bf/Y0[15] (butterfly_pe_q15)                           0.00       3.37 r
U437/Z (AO222D0)                                         0.07       3.44 r
u_memA/din[15] (sram_wrapper_1)                          0.00       3.44 r
u_memA/u_sram/D[15] (sram1024x32)                        0.00       3.44 r
data arrival time                                                   3.44

clock clk (rise edge)                                   10.00      10.00
clock network delay (ideal)                              0.00      10.00
clock uncertainty                                       -0.10       9.90
u_memA/u_sram/CLK (sram1024x32)                          0.00       9.90 r
library setup time                                      -0.09       9.81
data required time                                                  9.81
--------------------------------------------------------------------------
data required time                                                  9.81
data arrival time                                                  -3.44
--------------------------------------------------------------------------
slack (MET)                                                         6.37


Startpoint: w_reg_reg[17]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: u_memB/u_sram
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
sram_wrapper_0     ZeroWireload          tcbn65gplustc_ccs
sram_wrapper_1     ZeroWireload          tcbn65gplustc_ccs
fft1024_top        ZeroWireload          tcbn65gplustc_ccs
fft1024_controller ZeroWireload          tcbn65gplustc_ccs
complex_mult_q15   ZeroWireload          tcbn65gplustc_ccs
butterfly_pe_q15   ZeroWireload          tcbn65gplustc_ccs

Point                                                    Incr       Path
--------------------------------------------------------------------------
clock clk (rise edge)                                    0.00       0.00
clock network delay (ideal)                              0.00       0.00
w_reg_reg[17]/CP (DFCNQD1)                               0.00       0.00 r
w_reg_reg[17]/Q (DFCNQD1)                                0.09       0.09 r
```

```
u_bf/W[17] (butterfly_pe_q15)                          0.00       0.09 r
u_bf/u_mult/ar[1] (complex_mult_q15)                   0.00       0.09 r
u_bf/u_mult/U211/ZN (INVD0)                            0.04       0.13 f
u_bf/u_mult/U216/ZN (AOI22D0)                          0.12       0.25 r
u_bf/u_mult/U292/ZN (INVD0)                            0.05       0.30 f
u_bf/u_mult/U294/Z (OR2D0)                             0.06       0.36 f
u_bf/u_mult/U295/ZN (INVD0)                            0.13       0.49 r
u_bf/u_mult/U1197/ZN (AOI22D0)                         0.05       0.55 f
u_bf/u_mult/U1198/ZN (OAI221D0)                        0.05       0.60 r
u_bf/u_mult/DP_OP_7J2_125_8831/U272/S (CMPE42D1)       0.17       0.77 f
u_bf/u_mult/U838/ZN (MAOI222D0)                        0.06       0.82 r
u_bf/u_mult/U839/ZN (INVD0)                            0.02       0.84 f
u_bf/u_mult/U840/ZN (MAOI222D0)                        0.06       0.90 r
u_bf/u_mult/U841/ZN (INVD0)                            0.02       0.93 f
u_bf/u_mult/U842/ZN (MAOI222D0)                        0.06       0.98 r
u_bf/u_mult/U843/ZN (INVD0)                            0.02       1.00 f
u_bf/u_mult/U844/ZN (MAOI222D0)                        0.06       1.06 r
u_bf/u_mult/U845/ZN (INVD0)                            0.02       1.09 f
u_bf/u_mult/U846/ZN (MAOI222D0)                        0.06       1.14 r
u_bf/u_mult/U847/ZN (INVD0)                            0.02       1.16 f
u_bf/u_mult/U848/ZN (MAOI222D0)                        0.06       1.22 r
u_bf/u_mult/U849/ZN (INVD0)                            0.02       1.24 f
u_bf/u_mult/U850/ZN (MAOI222D0)                        0.06       1.30 r
u_bf/u_mult/U851/ZN (INVD0)                            0.02       1.32 f
u_bf/u_mult/U852/ZN (MAOI222D0)                        0.06       1.38 r
u_bf/u_mult/U853/ZN (INVD0)                            0.02       1.40 f
u_bf/u_mult/U854/ZN (MAOI222D0)                        0.06       1.46 r
u_bf/u_mult/U855/ZN (INVD0)                            0.02       1.48 f
u_bf/u_mult/U856/ZN (MAOI222D0)                        0.06       1.54 r
u_bf/u_mult/U857/ZN (INVD0)                            0.02       1.56 f
u_bf/u_mult/U858/ZN (MAOI222D0)                        0.06       1.62 r
u_bf/u_mult/U859/ZN (INVD0)                            0.02       1.64 f
u_bf/u_mult/U860/ZN (MAOI222D0)                        0.06       1.70 r
u_bf/u_mult/U861/ZN (INVD0)                            0.02       1.72 f
u_bf/u_mult/intadd_2/U16/CO (FA1D0)                    0.06       1.78 f
u_bf/u_mult/intadd_2/U15/S (FA1D0)                     0.07       1.85 f
u_bf/u_mult/pr[1] (complex_mult_q15)                   0.00       1.85 f
u_bf/U47/ZN (MAOI222D0)                                0.07       1.92 r
u_bf/U48/ZN (INVD0)                                    0.03       1.96 f
u_bf/U49/ZN (MAOI222D0)                                0.07       2.03 r
u_bf/U50/ZN (INVD0)                                    0.03       2.05 f
u_bf/U51/ZN (MAOI222D0)                                0.07       2.13 r
u_bf/U52/ZN (INVD0)                                    0.03       2.16 f
u_bf/U53/ZN (MAOI222D0)                                0.07       2.23 r
u_bf/U54/ZN (INVD0)                                    0.03       2.26 f
u_bf/U55/ZN (MAOI222D0)                                0.07       2.34 r
u_bf/U56/ZN (INVD0)                                    0.03       2.37 f
u_bf/U57/ZN (MAOI222D0)                                0.07       2.44 r
u_bf/U58/ZN (INVD0)                                    0.03       2.47 f
u_bf/U59/ZN (MAOI222D0)                                0.07       2.54 r
```

```
u_bf/U60/ZN (INVD0)                                      0.03       2.57 f
u_bf/U61/ZN (MAOI222D0)                                  0.07       2.64 r
u_bf/U62/ZN (INVD0)                                      0.03       2.67 f
u_bf/U63/ZN (MAOI222D0)                                  0.07       2.75 r
u_bf/U64/ZN (INVD0)                                      0.03       2.78 f
u_bf/U65/ZN (MAOI222D0)                                  0.07       2.85 r
u_bf/U66/ZN (INVD0)                                      0.03       2.88 f
u_bf/U67/ZN (MAOI222D0)                                  0.07       2.95 r
u_bf/U68/ZN (INVD0)                                      0.03       2.98 f
u_bf/U69/ZN (MAOI222D0)                                  0.07       3.05 r
u_bf/U70/ZN (INVD0)                                      0.03       3.08 f
u_bf/U71/ZN (MAOI222D0)                                  0.07       3.16 r
u_bf/U72/ZN (INVD0)                                      0.03       3.19 f
u_bf/U73/ZN (MAOI222D0)                                  0.07       3.26 r
u_bf/U74/ZN (INVD0)                                      0.03       3.29 f
u_bf/U75/ZN (MAOI222D0)                                  0.08       3.37 r
u_bf/Y0[31] (butterfly_pe_q15)                           0.00       3.37 r
U434/Z (AO222D0)                                         0.07       3.44 r
u_memB/din[31] (sram_wrapper_0)                          0.00       3.44 r
u_memB/u_sram/D[31] (sram1024x32)                        0.00       3.44 r
data arrival time                                                   3.44

clock clk (rise edge)                                   10.00      10.00
clock network delay (ideal)                              0.00      10.00
clock uncertainty                                       -0.10       9.90
u_memB/u_sram/CLK (sram1024x32)                          0.00       9.90 r
library setup time                                      -0.09       9.81
data required time                                                  9.81
--------------------------------------------------------------------------
data required time                                                  9.81
data arrival time                                                  -3.44
--------------------------------------------------------------------------
slack (MET)                                                         6.37


Startpoint: w_reg_reg[17]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: u_memB/u_sram
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
sram_wrapper_0     ZeroWireload          tcbn65gplustc_ccs
sram_wrapper_1     ZeroWireload          tcbn65gplustc_ccs
fft1024_top        ZeroWireload          tcbn65gplustc_ccs
fft1024_controller ZeroWireload          tcbn65gplustc_ccs
complex_mult_q15   ZeroWireload          tcbn65gplustc_ccs
butterfly_pe_q15   ZeroWireload          tcbn65gplustc_ccs
```

```
Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.00       0.00
w_reg_reg[17]/CP (DFCNQD1)                              0.00       0.00 r
w_reg_reg[17]/Q (DFCNQD1)                               0.09       0.09 r
u_bf/W[17] (butterfly_pe_q15)                           0.00       0.09 r
u_bf/u_mult/ar[1] (complex_mult_q15)                    0.00       0.09 r
u_bf/u_mult/U211/ZN (INVD0)                             0.04       0.13 f
u_bf/u_mult/U216/ZN (AOI22D0)                           0.12       0.25 r
u_bf/u_mult/U292/ZN (INVD0)                             0.05       0.30 f
u_bf/u_mult/U294/Z (OR2D0)                              0.06       0.36 f
u_bf/u_mult/U295/ZN (INVD0)                             0.13       0.49 r
u_bf/u_mult/U1487/ZN (AOI22D0)                          0.05       0.55 f
u_bf/u_mult/U1488/ZN (OAI221D0)                         0.05       0.60 r
u_bf/u_mult/DP_OP_8J2_126_8831/U272/S (CMPE42D1)        0.17       0.77 f
u_bf/u_mult/U887/ZN (MAOI222D0)                         0.06       0.82 r
u_bf/u_mult/U888/ZN (INVD0)                             0.02       0.84 f
u_bf/u_mult/U889/ZN (MAOI222D0)                         0.06       0.90 r
u_bf/u_mult/U890/ZN (INVD0)                             0.02       0.93 f
u_bf/u_mult/U891/ZN (MAOI222D0)                         0.06       0.98 r
u_bf/u_mult/U892/ZN (INVD0)                             0.02       1.00 f
u_bf/u_mult/U893/ZN (MAOI222D0)                         0.06       1.06 r
u_bf/u_mult/U894/ZN (INVD0)                             0.02       1.09 f
u_bf/u_mult/U895/ZN (MAOI222D0)                         0.06       1.14 r
u_bf/u_mult/U896/ZN (INVD0)                             0.02       1.16 f
u_bf/u_mult/U897/ZN (MAOI222D0)                         0.06       1.22 r
u_bf/u_mult/U898/ZN (INVD0)                             0.02       1.24 f
u_bf/u_mult/U899/ZN (MAOI222D0)                         0.06       1.30 r
u_bf/u_mult/U900/ZN (INVD0)                             0.02       1.32 f
u_bf/u_mult/U901/ZN (MAOI222D0)                         0.06       1.38 r
u_bf/u_mult/U902/ZN (INVD0)                             0.02       1.40 f
u_bf/u_mult/U903/ZN (MAOI222D0)                         0.06       1.46 r
u_bf/u_mult/U904/ZN (INVD0)                             0.02       1.48 f
u_bf/u_mult/U905/ZN (MAOI222D0)                         0.06       1.54 r
u_bf/u_mult/U906/ZN (INVD0)                             0.02       1.56 f
u_bf/u_mult/U907/ZN (MAOI222D0)                         0.06       1.62 r
u_bf/u_mult/U908/ZN (INVD0)                             0.02       1.64 f
u_bf/u_mult/U909/ZN (MAOI222D0)                         0.06       1.70 r
u_bf/u_mult/U910/ZN (INVD0)                             0.02       1.72 f
u_bf/u_mult/intadd_1/U16/CO (FA1D0)                     0.06       1.78 f
u_bf/u_mult/intadd_1/U15/S (FA1D0)                      0.07       1.85 f
u_bf/u_mult/pi[1] (complex_mult_q15)                    0.00       1.85 f
u_bf/U122/ZN (MAOI222D0)                                0.07       1.92 r
u_bf/U123/ZN (INVD0)                                    0.03       1.96 f
u_bf/U124/ZN (MAOI222D0)                                0.07       2.03 r
u_bf/U125/ZN (INVD0)                                    0.03       2.05 f
u_bf/U126/ZN (MAOI222D0)                                0.07       2.13 r
u_bf/U127/ZN (INVD0)                                    0.03       2.16 f
```

```
u_bf/U128/ZN (MAOI222D0)                                 0.07       2.23 r
u_bf/U129/ZN (INVD0)                                     0.03       2.26 f
u_bf/U130/ZN (MAOI222D0)                                 0.07       2.34 r
u_bf/U131/ZN (INVD0)                                     0.03       2.37 f
u_bf/U132/ZN (MAOI222D0)                                 0.07       2.44 r
u_bf/U133/ZN (INVD0)                                     0.03       2.47 f
u_bf/U134/ZN (MAOI222D0)                                 0.07       2.54 r
u_bf/U135/ZN (INVD0)                                     0.03       2.57 f
u_bf/U136/ZN (MAOI222D0)                                 0.07       2.64 r
u_bf/U137/ZN (INVD0)                                     0.03       2.67 f
u_bf/U138/ZN (MAOI222D0)                                 0.07       2.75 r
u_bf/U139/ZN (INVD0)                                     0.03       2.78 f
u_bf/U140/ZN (MAOI222D0)                                 0.07       2.85 r
u_bf/U141/ZN (INVD0)                                     0.03       2.88 f
u_bf/U142/ZN (MAOI222D0)                                 0.07       2.95 r
u_bf/U143/ZN (INVD0)                                     0.03       2.98 f
u_bf/U144/ZN (MAOI222D0)                                 0.07       3.05 r
u_bf/U145/ZN (INVD0)                                     0.03       3.08 f
u_bf/U146/ZN (MAOI222D0)                                 0.07       3.16 r
u_bf/U147/ZN (INVD0)                                     0.03       3.19 f
u_bf/U148/ZN (MAOI222D0)                                 0.07       3.26 r
u_bf/U149/ZN (INVD0)                                     0.03       3.29 f
u_bf/U150/ZN (MAOI222D0)                                 0.08       3.37 r
u_bf/Y0[15] (butterfly_pe_q15)                           0.00       3.37 r
U435/Z (AO222D0)                                         0.07       3.44 r
u_memB/din[15] (sram_wrapper_0)                          0.00       3.44 r
u_memB/u_sram/D[15] (sram1024x32)                        0.00       3.44 r
data arrival time                                                   3.44

clock clk (rise edge)                                   10.00      10.00
clock network delay (ideal)                              0.00      10.00
clock uncertainty                                       -0.10       9.90
u_memB/u_sram/CLK (sram1024x32)                          0.00       9.90 r
library setup time                                      -0.09       9.81
data required time                                                  9.81
--------------------------------------------------------------------------
data required time                                                  9.81
data arrival time                                                  -3.44
--------------------------------------------------------------------------
slack (MET)                                                         6.37


Startpoint: w_reg_reg[17]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: u_memB/u_sram
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
```

```
-------------------------------------------------
sram_wrapper_0     ZeroWireload          tcbn65gplustc_ccs
sram_wrapper_1     ZeroWireload          tcbn65gplustc_ccs
fft1024_top        ZeroWireload          tcbn65gplustc_ccs
fft1024_controller ZeroWireload          tcbn65gplustc_ccs
complex_mult_q15   ZeroWireload          tcbn65gplustc_ccs
butterfly_pe_q15   ZeroWireload          tcbn65gplustc_ccs

Point                                                       Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                       0.00       0.00
clock network delay (ideal)                                 0.00       0.00
w_reg_reg[17]/CP (DFCNQD1)                                  0.00       0.00 r
w_reg_reg[17]/Q (DFCNQD1)                                   0.09       0.09 r
u_bf/W[17] (butterfly_pe_q15)                               0.00       0.09 r
u_bf/u_mult/ar[1] (complex_mult_q15)                        0.00       0.09 r
u_bf/u_mult/U211/ZN (INVD0)                                 0.04       0.13 f
u_bf/u_mult/U216/ZN (AOI22D0)                               0.12       0.25 r
u_bf/u_mult/U292/ZN (INVD0)                                 0.05       0.30 f
u_bf/u_mult/U294/Z (OR2D0)                                  0.06       0.36 f
u_bf/u_mult/U295/ZN (INVD0)                                 0.13       0.49 r
u_bf/u_mult/U1197/ZN (AOI22D0)                              0.05       0.55 f
u_bf/u_mult/U1198/ZN (OAI221D0)                             0.05       0.60 r
u_bf/u_mult/DP_OP_7J2_125_8831/U272/S (CMPE42D1)            0.17       0.77 f
u_bf/u_mult/U838/ZN (MAOI222D0)                             0.06       0.82 r
u_bf/u_mult/U839/ZN (INVD0)                                 0.02       0.84 f
u_bf/u_mult/U840/ZN (MAOI222D0)                             0.06       0.90 r
u_bf/u_mult/U841/ZN (INVD0)                                 0.02       0.93 f
u_bf/u_mult/U842/ZN (MAOI222D0)                             0.06       0.98 r
u_bf/u_mult/U843/ZN (INVD0)                                 0.02       1.00 f
u_bf/u_mult/U844/ZN (MAOI222D0)                             0.06       1.06 r
u_bf/u_mult/U845/ZN (INVD0)                                 0.02       1.09 f
u_bf/u_mult/U846/ZN (MAOI222D0)                             0.06       1.14 r
u_bf/u_mult/U847/ZN (INVD0)                                 0.02       1.16 f
u_bf/u_mult/U848/ZN (MAOI222D0)                             0.06       1.22 r
u_bf/u_mult/U849/ZN (INVD0)                                 0.02       1.24 f
u_bf/u_mult/U850/ZN (MAOI222D0)                             0.06       1.30 r
u_bf/u_mult/U851/ZN (INVD0)                                 0.02       1.32 f
u_bf/u_mult/U852/ZN (MAOI222D0)                             0.06       1.38 r
u_bf/u_mult/U853/ZN (INVD0)                                 0.02       1.40 f
u_bf/u_mult/U854/ZN (MAOI222D0)                             0.06       1.46 r
u_bf/u_mult/U855/ZN (INVD0)                                 0.02       1.48 f
u_bf/u_mult/U856/ZN (MAOI222D0)                             0.06       1.54 r
u_bf/u_mult/U857/ZN (INVD0)                                 0.02       1.56 f
u_bf/u_mult/U858/ZN (MAOI222D0)                             0.06       1.62 r
u_bf/u_mult/U859/ZN (INVD0)                                 0.02       1.64 f
u_bf/u_mult/U860/ZN (MAOI222D0)                             0.06       1.70 r
u_bf/u_mult/U861/ZN (INVD0)                                 0.02       1.72 f
u_bf/u_mult/intadd_2/U16/CO (FA1D0)                         0.06       1.78 f
u_bf/u_mult/intadd_2/U15/S (FA1D0)                          0.07       1.85 f
```

```
u_bf/u_mult/pr[1] (complex_mult_q15)                    0.00       1.85 f
u_bf/U47/ZN (MAOI222D0)                                 0.07       1.92 r
u_bf/U48/ZN (INVD0)                                     0.03       1.96 f
u_bf/U49/ZN (MAOI222D0)                                 0.07       2.03 r
u_bf/U50/ZN (INVD0)                                     0.03       2.05 f
u_bf/U51/ZN (MAOI222D0)                                 0.07       2.13 r
u_bf/U52/ZN (INVD0)                                     0.03       2.16 f
u_bf/U53/ZN (MAOI222D0)                                 0.07       2.23 r
u_bf/U54/ZN (INVD0)                                     0.03       2.26 f
u_bf/U55/ZN (MAOI222D0)                                 0.07       2.34 r
u_bf/U56/ZN (INVD0)                                     0.03       2.37 f
u_bf/U57/ZN (MAOI222D0)                                 0.07       2.44 r
u_bf/U58/ZN (INVD0)                                     0.03       2.47 f
u_bf/U59/ZN (MAOI222D0)                                 0.07       2.54 r
u_bf/U60/ZN (INVD0)                                     0.03       2.57 f
u_bf/U61/ZN (MAOI222D0)                                 0.07       2.64 r
u_bf/U62/ZN (INVD0)                                     0.03       2.67 f
u_bf/U63/ZN (MAOI222D0)                                 0.07       2.75 r
u_bf/U64/ZN (INVD0)                                     0.03       2.78 f
u_bf/U65/ZN (MAOI222D0)                                 0.07       2.85 r
u_bf/U66/ZN (INVD0)                                     0.03       2.88 f
u_bf/U67/ZN (MAOI222D0)                                 0.07       2.95 r
u_bf/U68/ZN (INVD0)                                     0.03       2.98 f
u_bf/U69/ZN (MAOI222D0)                                 0.07       3.05 r
u_bf/U70/ZN (INVD0)                                     0.03       3.08 f
u_bf/U71/ZN (MAOI222D0)                                 0.07       3.16 r
u_bf/U72/ZN (INVD0)                                     0.03       3.19 f
u_bf/U73/ZN (MAOI222D0)                                 0.07       3.26 r
u_bf/U152/ZN (MUX2ND0)                                  0.04       3.30 f
u_bf/Y0[30] (butterfly_pe_q15)                          0.00       3.30 f
U432/Z (AO222D0)                                        0.11       3.41 f
u_memB/din[30] (sram_wrapper_0)                         0.00       3.41 f
u_memB/u_sram/D[30] (sram1024x32)                       0.00       3.41 f
data arrival time                                                  3.41

clock clk (rise edge)                                  10.00      10.00
clock network delay (ideal)                             0.00      10.00
clock uncertainty                                      -0.10       9.90
u_memB/u_sram/CLK (sram1024x32)                         0.00       9.90 r
library setup time                                     -0.10       9.80
data required time                                                 9.80
--------------------------------------------------------------------------
data required time                                                 9.80
data arrival time                                                 -3.41
--------------------------------------------------------------------------
slack (MET)                                                        6.39


Startpoint: w_reg_reg[17]
            (rising edge-triggered flip-flop clocked by clk)
```

```
Endpoint: u_memB/u_sram
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
sram_wrapper_0     ZeroWireload          tcbn65gplustc_ccs
sram_wrapper_1     ZeroWireload          tcbn65gplustc_ccs
fft1024_top        ZeroWireload          tcbn65gplustc_ccs
fft1024_controller ZeroWireload          tcbn65gplustc_ccs
complex_mult_q15   ZeroWireload          tcbn65gplustc_ccs
butterfly_pe_q15   ZeroWireload          tcbn65gplustc_ccs

Point                                                        Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                        0.00       0.00
clock network delay (ideal)                                  0.00       0.00
w_reg_reg[17]/CP (DFCNQD1)                                   0.00       0.00 r
w_reg_reg[17]/Q (DFCNQD1)                                    0.09       0.09 r
u_bf/W[17] (butterfly_pe_q15)                                0.00       0.09 r
u_bf/u_mult/ar[1] (complex_mult_q15)                         0.00       0.09 r
u_bf/u_mult/U211/ZN (INVD0)                                  0.04       0.13 f
u_bf/u_mult/U216/ZN (AOI22D0)                                0.12       0.25 r
u_bf/u_mult/U292/ZN (INVD0)                                  0.05       0.30 f
u_bf/u_mult/U294/Z (OR2D0)                                   0.06       0.36 f
u_bf/u_mult/U295/ZN (INVD0)                                  0.13       0.49 r
u_bf/u_mult/U1487/ZN (AOI22D0)                               0.05       0.55 f
u_bf/u_mult/U1488/ZN (OAI221D0)                              0.05       0.60 r
u_bf/u_mult/DP_OP_8J2_126_8831/U272/S (CMPE42D1)             0.17       0.77 f
u_bf/u_mult/U887/ZN (MAOI222D0)                              0.06       0.82 r
u_bf/u_mult/U888/ZN (INVD0)                                  0.02       0.84 f
u_bf/u_mult/U889/ZN (MAOI222D0)                              0.06       0.90 r
u_bf/u_mult/U890/ZN (INVD0)                                  0.02       0.93 f
u_bf/u_mult/U891/ZN (MAOI222D0)                              0.06       0.98 r
u_bf/u_mult/U892/ZN (INVD0)                                  0.02       1.00 f
u_bf/u_mult/U893/ZN (MAOI222D0)                              0.06       1.06 r
u_bf/u_mult/U894/ZN (INVD0)                                  0.02       1.09 f
u_bf/u_mult/U895/ZN (MAOI222D0)                              0.06       1.14 r
u_bf/u_mult/U896/ZN (INVD0)                                  0.02       1.16 f
u_bf/u_mult/U897/ZN (MAOI222D0)                              0.06       1.22 r
u_bf/u_mult/U898/ZN (INVD0)                                  0.02       1.24 f
u_bf/u_mult/U899/ZN (MAOI222D0)                              0.06       1.30 r
u_bf/u_mult/U900/ZN (INVD0)                                  0.02       1.32 f
u_bf/u_mult/U901/ZN (MAOI222D0)                              0.06       1.38 r
u_bf/u_mult/U902/ZN (INVD0)                                  0.02       1.40 f
u_bf/u_mult/U903/ZN (MAOI222D0)                              0.06       1.46 r
u_bf/u_mult/U904/ZN (INVD0)                                  0.02       1.48 f
u_bf/u_mult/U905/ZN (MAOI222D0)                              0.06       1.54 r
u_bf/u_mult/U906/ZN (INVD0)                                  0.02       1.56 f
```

```
u_bf/u_mult/U907/ZN (MAOI222D0)                          0.06       1.62 r
u_bf/u_mult/U908/ZN (INVD0)                              0.02       1.64 f
u_bf/u_mult/U909/ZN (MAOI222D0)                          0.06       1.70 r
u_bf/u_mult/U910/ZN (INVD0)                              0.02       1.72 f
u_bf/u_mult/intadd_1/U16/CO (FA1D0)                      0.06       1.78 f
u_bf/u_mult/intadd_1/U15/S (FA1D0)                       0.07       1.85 f
u_bf/u_mult/pi[1] (complex_mult_q15)                     0.00       1.85 f
u_bf/U122/ZN (MAOI222D0)                                 0.07       1.92 r
u_bf/U123/ZN (INVD0)                                     0.03       1.96 f
u_bf/U124/ZN (MAOI222D0)                                 0.07       2.03 r
u_bf/U125/ZN (INVD0)                                     0.03       2.05 f
u_bf/U126/ZN (MAOI222D0)                                 0.07       2.13 r
u_bf/U127/ZN (INVD0)                                     0.03       2.16 f
u_bf/U128/ZN (MAOI222D0)                                 0.07       2.23 r
u_bf/U129/ZN (INVD0)                                     0.03       2.26 f
u_bf/U130/ZN (MAOI222D0)                                 0.07       2.34 r
u_bf/U131/ZN (INVD0)                                     0.03       2.37 f
u_bf/U132/ZN (MAOI222D0)                                 0.07       2.44 r
u_bf/U133/ZN (INVD0)                                     0.03       2.47 f
u_bf/U134/ZN (MAOI222D0)                                 0.07       2.54 r
u_bf/U135/ZN (INVD0)                                     0.03       2.57 f
u_bf/U136/ZN (MAOI222D0)                                 0.07       2.64 r
u_bf/U137/ZN (INVD0)                                     0.03       2.67 f
u_bf/U138/ZN (MAOI222D0)                                 0.07       2.75 r
u_bf/U139/ZN (INVD0)                                     0.03       2.78 f
u_bf/U140/ZN (MAOI222D0)                                 0.07       2.85 r
u_bf/U141/ZN (INVD0)                                     0.03       2.88 f
u_bf/U142/ZN (MAOI222D0)                                 0.07       2.95 r
u_bf/U143/ZN (INVD0)                                     0.03       2.98 f
u_bf/U144/ZN (MAOI222D0)                                 0.07       3.05 r
u_bf/U145/ZN (INVD0)                                     0.03       3.08 f
u_bf/U146/ZN (MAOI222D0)                                 0.07       3.16 r
u_bf/U147/ZN (INVD0)                                     0.03       3.19 f
u_bf/U148/ZN (MAOI222D0)                                 0.07       3.26 r
u_bf/U184/ZN (MUX2ND0)                                   0.04       3.30 f
u_bf/Y0[14] (butterfly_pe_q15)                           0.00       3.30 f
U433/Z (AO222D0)                                         0.11       3.41 f
u_memB/din[14] (sram_wrapper_0)                          0.00       3.41 f
u_memB/u_sram/D[14] (sram1024x32)                        0.00       3.41 f
data arrival time                                                   3.41

clock clk (rise edge)                                   10.00      10.00
clock network delay (ideal)                              0.00      10.00
clock uncertainty                                       -0.10       9.90
u_memB/u_sram/CLK (sram1024x32)                          0.00       9.90 r
library setup time                                      -0.10       9.80
data required time                                                  9.80
--------------------------------------------------------------------------
data required time                                                  9.80
data arrival time                                                  -3.41
```

```
--------------------------------------------------------------------------------
slack (MET)                                                             6.39


Startpoint: w_reg_reg[17]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: u_memA/u_sram
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
sram_wrapper_0     ZeroWireload          tcbn65gplustc_ccs
sram_wrapper_1     ZeroWireload          tcbn65gplustc_ccs
fft1024_top        ZeroWireload          tcbn65gplustc_ccs
fft1024_controller ZeroWireload          tcbn65gplustc_ccs
complex_mult_q15   ZeroWireload          tcbn65gplustc_ccs
butterfly_pe_q15   ZeroWireload          tcbn65gplustc_ccs

Point                                                   Incr       Path
--------------------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.00       0.00
w_reg_reg[17]/CP (DFCNQD1)                              0.00       0.00 r
w_reg_reg[17]/Q (DFCNQD1)                               0.09       0.09 r
u_bf/W[17] (butterfly_pe_q15)                           0.00       0.09 r
u_bf/u_mult/ar[1] (complex_mult_q15)                    0.00       0.09 r
u_bf/u_mult/U211/ZN (INVD0)                             0.04       0.13 f
u_bf/u_mult/U216/ZN (AOI22D0)                           0.12       0.25 r
u_bf/u_mult/U292/ZN (INVD0)                             0.05       0.30 f
u_bf/u_mult/U294/Z (OR2D0)                              0.06       0.36 f
u_bf/u_mult/U295/ZN (INVD0)                             0.13       0.49 r
u_bf/u_mult/U1197/ZN (AOI22D0)                          0.05       0.55 f
u_bf/u_mult/U1198/ZN (OAI221D0)                         0.05       0.60 r
u_bf/u_mult/DP_OP_7J2_125_8831/U272/S (CMPE42D1)        0.17       0.77 f
u_bf/u_mult/U838/ZN (MAOI222D0)                         0.06       0.82 r
u_bf/u_mult/U839/ZN (INVD0)                             0.02       0.84 f
u_bf/u_mult/U840/ZN (MAOI222D0)                         0.06       0.90 r
u_bf/u_mult/U841/ZN (INVD0)                             0.02       0.93 f
u_bf/u_mult/U842/ZN (MAOI222D0)                         0.06       0.98 r
u_bf/u_mult/U843/ZN (INVD0)                             0.02       1.00 f
u_bf/u_mult/U844/ZN (MAOI222D0)                         0.06       1.06 r
u_bf/u_mult/U845/ZN (INVD0)                             0.02       1.09 f
u_bf/u_mult/U846/ZN (MAOI222D0)                         0.06       1.14 r
u_bf/u_mult/U847/ZN (INVD0)                             0.02       1.16 f
u_bf/u_mult/U848/ZN (MAOI222D0)                         0.06       1.22 r
u_bf/u_mult/U849/ZN (INVD0)                             0.02       1.24 f
u_bf/u_mult/U850/ZN (MAOI222D0)                         0.06       1.30 r
u_bf/u_mult/U851/ZN (INVD0)                             0.02       1.32 f
```

```
u_bf/u_mult/U852/ZN (MAOI222D0)                          0.06       1.38 r
u_bf/u_mult/U853/ZN (INVD0)                              0.02       1.40 f
u_bf/u_mult/U854/ZN (MAOI222D0)                          0.06       1.46 r
u_bf/u_mult/U855/ZN (INVD0)                              0.02       1.48 f
u_bf/u_mult/U856/ZN (MAOI222D0)                          0.06       1.54 r
u_bf/u_mult/U857/ZN (INVD0)                              0.02       1.56 f
u_bf/u_mult/U858/ZN (MAOI222D0)                          0.06       1.62 r
u_bf/u_mult/U859/ZN (INVD0)                              0.02       1.64 f
u_bf/u_mult/U860/ZN (MAOI222D0)                          0.06       1.70 r
u_bf/u_mult/U861/ZN (INVD0)                              0.02       1.72 f
u_bf/u_mult/intadd_2/U16/CO (FA1D0)                      0.06       1.78 f
u_bf/u_mult/intadd_2/U15/S (FA1D0)                       0.07       1.85 f
u_bf/u_mult/pr[1] (complex_mult_q15)                     0.00       1.85 f
u_bf/U47/ZN (MAOI222D0)                                  0.07       1.92 r
u_bf/U48/ZN (INVD0)                                      0.03       1.96 f
u_bf/U49/ZN (MAOI222D0)                                  0.07       2.03 r
u_bf/U50/ZN (INVD0)                                      0.03       2.05 f
u_bf/U51/ZN (MAOI222D0)                                  0.07       2.13 r
u_bf/U52/ZN (INVD0)                                      0.03       2.16 f
u_bf/U53/ZN (MAOI222D0)                                  0.07       2.23 r
u_bf/U54/ZN (INVD0)                                      0.03       2.26 f
u_bf/U55/ZN (MAOI222D0)                                  0.07       2.34 r
u_bf/U56/ZN (INVD0)                                      0.03       2.37 f
u_bf/U57/ZN (MAOI222D0)                                  0.07       2.44 r
u_bf/U58/ZN (INVD0)                                      0.03       2.47 f
u_bf/U59/ZN (MAOI222D0)                                  0.07       2.54 r
u_bf/U60/ZN (INVD0)                                      0.03       2.57 f
u_bf/U61/ZN (MAOI222D0)                                  0.07       2.64 r
u_bf/U62/ZN (INVD0)                                      0.03       2.67 f
u_bf/U63/ZN (MAOI222D0)                                  0.07       2.75 r
u_bf/U64/ZN (INVD0)                                      0.03       2.78 f
u_bf/U65/ZN (MAOI222D0)                                  0.07       2.85 r
u_bf/U66/ZN (INVD0)                                      0.03       2.88 f
u_bf/U67/ZN (MAOI222D0)                                  0.07       2.95 r
u_bf/U68/ZN (INVD0)                                      0.03       2.98 f
u_bf/U69/ZN (MAOI222D0)                                  0.07       3.05 r
u_bf/U70/ZN (INVD0)                                      0.03       3.08 f
u_bf/U71/ZN (MAOI222D0)                                  0.07       3.16 r
u_bf/U72/ZN (INVD0)                                      0.03       3.19 f
u_bf/U73/ZN (MAOI222D0)                                  0.07       3.26 r
u_bf/U152/ZN (MUX2ND0)                                   0.04       3.30 f
u_bf/Y0[30] (butterfly_pe_q15)                           0.00       3.30 f
U430/Z (AO222D0)                                         0.11       3.41 f
u_memA/din[30] (sram_wrapper_1)                          0.00       3.41 f
u_memA/u_sram/D[30] (sram1024x32)                        0.00       3.41 f
data arrival time                                                   3.41

clock clk (rise edge)                                   10.00      10.00
clock network delay (ideal)                              0.00      10.00
clock uncertainty                                       -0.10       9.90
```

```
u_memA/u_sram/CLK (sram1024x32)                          0.00       9.90 r
library setup time                                      -0.10       9.80
data required time                                                  9.80
--------------------------------------------------------------------------
data required time                                                  9.80
data arrival time                                                  -3.41
--------------------------------------------------------------------------
slack (MET)                                                         6.39


Startpoint: w_reg_reg[17]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: u_memA/u_sram
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
sram_wrapper_0     ZeroWireload          tcbn65gplustc_ccs
sram_wrapper_1     ZeroWireload          tcbn65gplustc_ccs
fft1024_top        ZeroWireload          tcbn65gplustc_ccs
fft1024_controller ZeroWireload          tcbn65gplustc_ccs
complex_mult_q15   ZeroWireload          tcbn65gplustc_ccs
butterfly_pe_q15   ZeroWireload          tcbn65gplustc_ccs

Point                                                    Incr       Path
--------------------------------------------------------------------------
clock clk (rise edge)                                    0.00       0.00
clock network delay (ideal)                              0.00       0.00
w_reg_reg[17]/CP (DFCNQD1)                               0.00       0.00 r
w_reg_reg[17]/Q (DFCNQD1)                                0.09       0.09 r
u_bf/W[17] (butterfly_pe_q15)                            0.00       0.09 r
u_bf/u_mult/ar[1] (complex_mult_q15)                     0.00       0.09 r
u_bf/u_mult/U211/ZN (INVD0)                              0.04       0.13 f
u_bf/u_mult/U216/ZN (AOI22D0)                            0.12       0.25 r
u_bf/u_mult/U292/ZN (INVD0)                              0.05       0.30 f
u_bf/u_mult/U294/Z (OR2D0)                               0.06       0.36 f
u_bf/u_mult/U295/ZN (INVD0)                              0.13       0.49 r
u_bf/u_mult/U1487/ZN (AOI22D0)                           0.05       0.55 f
u_bf/u_mult/U1488/ZN (OAI221D0)                          0.05       0.60 r
u_bf/u_mult/DP_OP_8J2_126_8831/U272/S (CMPE42D1)         0.17       0.77 f
u_bf/u_mult/U887/ZN (MAOI222D0)                          0.06       0.82 r
u_bf/u_mult/U888/ZN (INVD0)                              0.02       0.84 f
u_bf/u_mult/U889/ZN (MAOI222D0)                          0.06       0.90 r
u_bf/u_mult/U890/ZN (INVD0)                              0.02       0.93 f
u_bf/u_mult/U891/ZN (MAOI222D0)                          0.06       0.98 r
u_bf/u_mult/U892/ZN (INVD0)                              0.02       1.00 f
u_bf/u_mult/U893/ZN (MAOI222D0)                          0.06       1.06 r
u_bf/u_mult/U894/ZN (INVD0)                              0.02       1.09 f
```

```
u_bf/u_mult/U895/ZN (MAOI222D0)                    0.06       1.14 r
u_bf/u_mult/U896/ZN (INVD0)                        0.02       1.16 f
u_bf/u_mult/U897/ZN (MAOI222D0)                    0.06       1.22 r
u_bf/u_mult/U898/ZN (INVD0)                        0.02       1.24 f
u_bf/u_mult/U899/ZN (MAOI222D0)                    0.06       1.30 r
u_bf/u_mult/U900/ZN (INVD0)                        0.02       1.32 f
u_bf/u_mult/U901/ZN (MAOI222D0)                    0.06       1.38 r
u_bf/u_mult/U902/ZN (INVD0)                        0.02       1.40 f
u_bf/u_mult/U903/ZN (MAOI222D0)                    0.06       1.46 r
u_bf/u_mult/U904/ZN (INVD0)                        0.02       1.48 f
u_bf/u_mult/U905/ZN (MAOI222D0)                    0.06       1.54 r
u_bf/u_mult/U906/ZN (INVD0)                        0.02       1.56 f
u_bf/u_mult/U907/ZN (MAOI222D0)                    0.06       1.62 r
u_bf/u_mult/U908/ZN (INVD0)                        0.02       1.64 f
u_bf/u_mult/U909/ZN (MAOI222D0)                    0.06       1.70 r
u_bf/u_mult/U910/ZN (INVD0)                        0.02       1.72 f
u_bf/u_mult/intadd_1/U16/CO (FA1D0)                0.06       1.78 f
u_bf/u_mult/intadd_1/U15/S (FA1D0)                 0.07       1.85 f
u_bf/u_mult/pi[1] (complex_mult_q15)               0.00       1.85 f
u_bf/U122/ZN (MAOI222D0)                           0.07       1.92 r
u_bf/U123/ZN (INVD0)                               0.03       1.96 f
u_bf/U124/ZN (MAOI222D0)                           0.07       2.03 r
u_bf/U125/ZN (INVD0)                               0.03       2.05 f
u_bf/U126/ZN (MAOI222D0)                           0.07       2.13 r
u_bf/U127/ZN (INVD0)                               0.03       2.16 f
u_bf/U128/ZN (MAOI222D0)                           0.07       2.23 r
u_bf/U129/ZN (INVD0)                               0.03       2.26 f
u_bf/U130/ZN (MAOI222D0)                           0.07       2.34 r
u_bf/U131/ZN (INVD0)                               0.03       2.37 f
u_bf/U132/ZN (MAOI222D0)                           0.07       2.44 r
u_bf/U133/ZN (INVD0)                               0.03       2.47 f
u_bf/U134/ZN (MAOI222D0)                           0.07       2.54 r
u_bf/U135/ZN (INVD0)                               0.03       2.57 f
u_bf/U136/ZN (MAOI222D0)                           0.07       2.64 r
u_bf/U137/ZN (INVD0)                               0.03       2.67 f
u_bf/U138/ZN (MAOI222D0)                           0.07       2.75 r
u_bf/U139/ZN (INVD0)                               0.03       2.78 f
u_bf/U140/ZN (MAOI222D0)                           0.07       2.85 r
u_bf/U141/ZN (INVD0)                               0.03       2.88 f
u_bf/U142/ZN (MAOI222D0)                           0.07       2.95 r
u_bf/U143/ZN (INVD0)                               0.03       2.98 f
u_bf/U144/ZN (MAOI222D0)                           0.07       3.05 r
u_bf/U145/ZN (INVD0)                               0.03       3.08 f
u_bf/U146/ZN (MAOI222D0)                           0.07       3.16 r
u_bf/U147/ZN (INVD0)                               0.03       3.19 f
u_bf/U148/ZN (MAOI222D0)                           0.07       3.26 r
u_bf/U184/ZN (MUX2ND0)                             0.04       3.30 f
u_bf/Y0[14] (butterfly_pe_q15)                     0.00       3.30 f
U431/Z (AO222D0)                                   0.11       3.41 f
u_memA/din[14] (sram_wrapper_1)                    0.00       3.41 f
```

```
u_memA/u_sram/D[14] (sram1024x32)                        0.00       3.41 f
data arrival time                                                   3.41

clock clk (rise edge)                                   10.00      10.00
clock network delay (ideal)                              0.00      10.00
clock uncertainty                                       -0.10       9.90
u_memA/u_sram/CLK (sram1024x32)                          0.00       9.90 r
library setup time                                      -0.10       9.80
data required time                                                  9.80
--------------------------------------------------------------------------
data required time                                                  9.80
data arrival time                                                  -3.41
--------------------------------------------------------------------------
slack (MET)                                                         6.39


Startpoint: w_reg_reg[17]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: u_memA/u_sram
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
sram_wrapper_0     ZeroWireload          tcbn65gplustc_ccs
sram_wrapper_1     ZeroWireload          tcbn65gplustc_ccs
fft1024_top        ZeroWireload          tcbn65gplustc_ccs
fft1024_controller ZeroWireload          tcbn65gplustc_ccs
complex_mult_q15   ZeroWireload          tcbn65gplustc_ccs
butterfly_pe_q15   ZeroWireload          tcbn65gplustc_ccs

Point                                                    Incr       Path
--------------------------------------------------------------------------
clock clk (rise edge)                                    0.00       0.00
clock network delay (ideal)                              0.00       0.00
w_reg_reg[17]/CP (DFCNQD1)                               0.00       0.00 r
w_reg_reg[17]/Q (DFCNQD1)                                0.09       0.09 r
u_bf/W[17] (butterfly_pe_q15)                            0.00       0.09 r
u_bf/u_mult/ar[1] (complex_mult_q15)                     0.00       0.09 r
u_bf/u_mult/U211/ZN (INVD0)                              0.04       0.13 f
u_bf/u_mult/U216/ZN (AOI22D0)                            0.12       0.25 r
u_bf/u_mult/U292/ZN (INVD0)                              0.05       0.30 f
u_bf/u_mult/U294/Z (OR2D0)                               0.06       0.36 f
u_bf/u_mult/U295/ZN (INVD0)                              0.13       0.49 r
u_bf/u_mult/U1487/ZN (AOI22D0)                           0.05       0.55 f
u_bf/u_mult/U1488/ZN (OAI221D0)                          0.05       0.60 r
u_bf/u_mult/DP_OP_8J2_126_8831/U272/S (CMPE42D1)         0.17       0.77 f
u_bf/u_mult/U887/ZN (MAOI222D0)                          0.06       0.82 r
u_bf/u_mult/U888/ZN (INVD0)                              0.02       0.84 f
```

```
u_bf/u_mult/U889/ZN (MAOI222D0)                    0.06       0.90 r
u_bf/u_mult/U890/ZN (INVD0)                        0.02       0.93 f
u_bf/u_mult/U891/ZN (MAOI222D0)                    0.06       0.98 r
u_bf/u_mult/U892/ZN (INVD0)                        0.02       1.00 f
u_bf/u_mult/U893/ZN (MAOI222D0)                    0.06       1.06 r
u_bf/u_mult/U894/ZN (INVD0)                        0.02       1.09 f
u_bf/u_mult/U895/ZN (MAOI222D0)                    0.06       1.14 r
u_bf/u_mult/U896/ZN (INVD0)                        0.02       1.16 f
u_bf/u_mult/U897/ZN (MAOI222D0)                    0.06       1.22 r
u_bf/u_mult/U898/ZN (INVD0)                        0.02       1.24 f
u_bf/u_mult/U899/ZN (MAOI222D0)                    0.06       1.30 r
u_bf/u_mult/U900/ZN (INVD0)                        0.02       1.32 f
u_bf/u_mult/U901/ZN (MAOI222D0)                    0.06       1.38 r
u_bf/u_mult/U902/ZN (INVD0)                        0.02       1.40 f
u_bf/u_mult/U903/ZN (MAOI222D0)                    0.06       1.46 r
u_bf/u_mult/U904/ZN (INVD0)                        0.02       1.48 f
u_bf/u_mult/U905/ZN (MAOI222D0)                    0.06       1.54 r
u_bf/u_mult/U906/ZN (INVD0)                        0.02       1.56 f
u_bf/u_mult/U907/ZN (MAOI222D0)                    0.06       1.62 r
u_bf/u_mult/U908/ZN (INVD0)                        0.02       1.64 f
u_bf/u_mult/U909/ZN (MAOI222D0)                    0.06       1.70 r
u_bf/u_mult/U910/ZN (INVD0)                        0.02       1.72 f
u_bf/u_mult/intadd_1/U16/CO (FA1D0)                0.06       1.78 f
u_bf/u_mult/intadd_1/U15/S (FA1D0)                 0.07       1.85 f
u_bf/u_mult/pi[1] (complex_mult_q15)               0.00       1.85 f
u_bf/U88/ZN (MAOI222D0)                            0.07       1.93 r
u_bf/U89/ZN (INVD0)                                0.03       1.96 f
u_bf/U91/ZN (MAOI222D0)                            0.07       2.03 r
u_bf/U92/ZN (INVD0)                                0.03       2.06 f
u_bf/U93/ZN (MAOI222D0)                            0.07       2.13 r
u_bf/U94/ZN (INVD0)                                0.03       2.17 f
u_bf/U96/ZN (MAOI222D0)                            0.07       2.24 r
u_bf/U97/ZN (INVD0)                                0.03       2.27 f
u_bf/U98/ZN (MAOI222D0)                            0.07       2.34 r
u_bf/U99/ZN (INVD0)                                0.03       2.37 f
u_bf/U101/ZN (MAOI222D0)                           0.07       2.45 r
u_bf/U102/ZN (INVD0)                               0.03       2.48 f
u_bf/U103/ZN (MAOI222D0)                           0.07       2.55 r
u_bf/U104/ZN (INVD0)                               0.03       2.58 f
u_bf/U106/ZN (MAOI222D0)                           0.07       2.66 r
u_bf/U107/ZN (INVD0)                               0.03       2.68 f
u_bf/U108/ZN (MAOI222D0)                           0.07       2.76 r
u_bf/U109/ZN (INVD0)                               0.03       2.79 f
u_bf/U111/ZN (MAOI222D0)                           0.07       2.86 r
u_bf/U112/ZN (INVD0)                               0.03       2.89 f
u_bf/U113/ZN (MAOI222D0)                           0.09       2.98 r
u_bf/U114/ZN (MAOI222D0)                           0.07       3.06 f
u_bf/U115/ZN (MAOI222D0)                           0.10       3.16 r
u_bf/U232/ZN (MUX2ND0)                             0.07       3.23 f
u_bf/Y1[13] (butterfly_pe_q15)                     0.00       3.23 f
```

```
U428/Z (AO222D0)                                          0.12       3.34 f
u_memA/din[13] (sram_wrapper_1)                           0.00       3.34 f
u_memA/u_sram/D[13] (sram1024x32)                         0.00       3.34 f
data arrival time                                                    3.34

clock clk (rise edge)                                    10.00      10.00
clock network delay (ideal)                               0.00      10.00
clock uncertainty                                        -0.10       9.90
u_memA/u_sram/CLK (sram1024x32)                           0.00       9.90 r
library setup time                                       -0.10       9.80
data required time                                                   9.80
--------------------------------------------------------------------------
data required time                                                   9.80
data arrival time                                                   -3.34
--------------------------------------------------------------------------
slack (MET)                                                          6.46


Startpoint: w_reg_reg[17]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: u_memA/u_sram
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
sram_wrapper_0     ZeroWireload          tcbn65gplustc_ccs
sram_wrapper_1     ZeroWireload          tcbn65gplustc_ccs
fft1024_top        ZeroWireload          tcbn65gplustc_ccs
fft1024_controller ZeroWireload          tcbn65gplustc_ccs
complex_mult_q15   ZeroWireload          tcbn65gplustc_ccs
butterfly_pe_q15   ZeroWireload          tcbn65gplustc_ccs

Point                                                     Incr       Path
--------------------------------------------------------------------------
clock clk (rise edge)                                     0.00       0.00
clock network delay (ideal)                               0.00       0.00
w_reg_reg[17]/CP (DFCNQD1)                                0.00       0.00 r
w_reg_reg[17]/Q (DFCNQD1)                                 0.09       0.09 r
u_bf/W[17] (butterfly_pe_q15)                             0.00       0.09 r
u_bf/u_mult/ar[1] (complex_mult_q15)                      0.00       0.09 r
u_bf/u_mult/U211/ZN (INVD0)                               0.04       0.13 f
u_bf/u_mult/U216/ZN (AOI22D0)                             0.12       0.25 r
u_bf/u_mult/U292/ZN (INVD0)                               0.05       0.30 f
u_bf/u_mult/U294/Z (OR2D0)                                0.06       0.36 f
u_bf/u_mult/U295/ZN (INVD0)                               0.13       0.49 r
u_bf/u_mult/U1197/ZN (AOI22D0)                            0.05       0.55 f
u_bf/u_mult/U1198/ZN (OAI221D0)                           0.05       0.60 r
u_bf/u_mult/DP_OP_7J2_125_8831/U272/S (CMPE42D1)          0.17       0.77 f
```

```
u_bf/u_mult/U838/ZN (MAOI222D0)                    0.06       0.82 r
u_bf/u_mult/U839/ZN (INVD0)                        0.02       0.84 f
u_bf/u_mult/U840/ZN (MAOI222D0)                    0.06       0.90 r
u_bf/u_mult/U841/ZN (INVD0)                        0.02       0.93 f
u_bf/u_mult/U842/ZN (MAOI222D0)                    0.06       0.98 r
u_bf/u_mult/U843/ZN (INVD0)                        0.02       1.00 f
u_bf/u_mult/U844/ZN (MAOI222D0)                    0.06       1.06 r
u_bf/u_mult/U845/ZN (INVD0)                        0.02       1.09 f
u_bf/u_mult/U846/ZN (MAOI222D0)                    0.06       1.14 r
u_bf/u_mult/U847/ZN (INVD0)                        0.02       1.16 f
u_bf/u_mult/U848/ZN (MAOI222D0)                    0.06       1.22 r
u_bf/u_mult/U849/ZN (INVD0)                        0.02       1.24 f
u_bf/u_mult/U850/ZN (MAOI222D0)                    0.06       1.30 r
u_bf/u_mult/U851/ZN (INVD0)                        0.02       1.32 f
u_bf/u_mult/U852/ZN (MAOI222D0)                    0.06       1.38 r
u_bf/u_mult/U853/ZN (INVD0)                        0.02       1.40 f
u_bf/u_mult/U854/ZN (MAOI222D0)                    0.06       1.46 r
u_bf/u_mult/U855/ZN (INVD0)                        0.02       1.48 f
u_bf/u_mult/U856/ZN (MAOI222D0)                    0.06       1.54 r
u_bf/u_mult/U857/ZN (INVD0)                        0.02       1.56 f
u_bf/u_mult/U858/ZN (MAOI222D0)                    0.06       1.62 r
u_bf/u_mult/U859/ZN (INVD0)                        0.02       1.64 f
u_bf/u_mult/U860/ZN (MAOI222D0)                    0.06       1.70 r
u_bf/u_mult/U861/ZN (INVD0)                        0.02       1.72 f
u_bf/u_mult/intadd_2/U16/CO (FA1D0)                0.06       1.78 f
u_bf/u_mult/intadd_2/U15/S (FA1D0)                 0.07       1.85 f
u_bf/u_mult/pr[1] (complex_mult_q15)               0.00       1.85 f
u_bf/U13/ZN (MAOI222D0)                            0.07       1.93 r
u_bf/U14/ZN (INVD0)                                0.03       1.96 f
u_bf/U16/ZN (MAOI222D0)                            0.07       2.03 r
u_bf/U17/ZN (INVD0)                                0.03       2.06 f
u_bf/U18/ZN (MAOI222D0)                            0.07       2.13 r
u_bf/U19/ZN (INVD0)                                0.03       2.17 f
u_bf/U21/ZN (MAOI222D0)                            0.07       2.24 r
u_bf/U22/ZN (INVD0)                                0.03       2.27 f
u_bf/U23/ZN (MAOI222D0)                            0.07       2.34 r
u_bf/U24/ZN (INVD0)                                0.03       2.37 f
u_bf/U26/ZN (MAOI222D0)                            0.07       2.45 r
u_bf/U27/ZN (INVD0)                                0.03       2.48 f
u_bf/U28/ZN (MAOI222D0)                            0.07       2.55 r
u_bf/U29/ZN (INVD0)                                0.03       2.58 f
u_bf/U31/ZN (MAOI222D0)                            0.07       2.66 r
u_bf/U32/ZN (INVD0)                                0.03       2.68 f
u_bf/U33/ZN (MAOI222D0)                            0.07       2.76 r
u_bf/U34/ZN (INVD0)                                0.03       2.79 f
u_bf/U36/ZN (MAOI222D0)                            0.07       2.86 r
u_bf/U37/ZN (INVD0)                                0.03       2.89 f
u_bf/U38/ZN (MAOI222D0)                            0.09       2.98 r
u_bf/U39/ZN (MAOI222D0)                            0.07       3.06 f
u_bf/U40/ZN (MAOI222D0)                            0.10       3.16 r
```

```
  u_bf/U216/ZN (MUX2ND0)                                  0.07       3.23 f
  u_bf/Y1[29] (butterfly_pe_q15)                          0.00       3.23 f
  U427/Z (AO222D0)                                        0.12       3.34 f
  u_memA/din[29] (sram_wrapper_1)                         0.00       3.34 f
  u_memA/u_sram/D[29] (sram1024x32)                       0.00       3.34 f
  data arrival time                                                  3.34

  clock clk (rise edge)                                  10.00      10.00
  clock network delay (ideal)                             0.00      10.00
  clock uncertainty                                      -0.10       9.90
  u_memA/u_sram/CLK (sram1024x32)                         0.00       9.90 r
  library setup time                                     -0.10       9.80
  data required time                                                 9.80
  ---------------------------------------------------------------------------
  data required time                                                 9.80
  data arrival time                                                 -3.34
  ---------------------------------------------------------------------------
  slack (MET)                                                        6.46


1
```

```
****************************************
Report : timing
         -path_type full_clock_expanded
         -delay_type min
         -slack_lesser_than 0.00
         -max_paths 10
         -sort_by slack
Design : fft1024_top
Version: U-2022.12-SP5
Date   : Fri Apr 17 12:28:01 2026
****************************************

No paths with slack less than 0.00.

1
```

```
****************************************
Report : timing
         -path_type full_clock_expanded
         -delay_type max
         -slack_lesser_than 0.00
         -max_paths 10
         -sort_by slack
Design : fft1024_top
Version: U-2022.12-SP5
Date   : Fri Apr 17 12:28:01 2026
****************************************

No paths with slack less than 0.00.

1
```