Design and Verification of a Fully Differential Switched-Capacitor Gain-of-Two Amplifier

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***Abstract*—This report presents the design and verification of a fully differential switched-capacitor amplifier for a 1.5-bit/stage pipelined ADC residue stage. The selected system target is a 4 MHz sampling frequency and 9-bit resolution. The circuit includes a fully differential two-stage OTA with Miller compensation, a switched-capacitor common-mode feedback network, MOS transmission-gate switches, and sampling capacitors. The OTA achieves a 90.86 dB DC gain, a 47.86 MHz unity-gain bandwidth, and an 80.32° phase margin. The complete switched-capacitor amplifier consumes approximately 450 µW from a 1.8 V supply, yielding a figure of merit of 0.220 pJ/conversion-step.**

***Index Terms*—switched-capacitor amplifier, fully differential OTA, common-mode feedback, pipelined ADC, sample-and-hold**

I. Introduction

This project designs a fully differential switched-capacitor sample-and-hold amplifier for a pipelined ADC residue stage. The complete circuit, shown in Fig. 1, contains the fully differential OTA, the switched-capacitor common-mode feedback (CMFB) network, the sampling and feedback capacitors, and the MOS transmission-gate switches controlled by the non-overlapping clock phases ϕ_s and ϕ_h. The target closed-loop gain is two. The design operates with a 1.8 V supply at a 4 MHz sampling frequency and targets 9-bit accuracy.

One of the main issues is reaching sufficient output accuracy within one clock phase while minimizing power consumption. The OTA needs enough DC gain to keep the static gain error small, and it must also have sufficient bandwidth so the output can settle fast enough. The phase margin must remain high to avoid instability during closed-loop operation. In the switched-capacitor stage, the capacitor ratios and switching behavior must support accurate charge transfer while keeping thermal noise, charge injection, and clock feedthrough under control.

The rest of this report is organized as follows. Section II discusses the system-level parameter choices and the constraint on the switch resistance. Section III derives the charge-domain transfer function of the switched-capacitor gain stage and discusses charge-injection effects. Section IV presents the OTA topology selection, the OTA specification derivation, the input-referred noise budget, and the common-mode feedback design. Section V shows the transient verification of the complete amplifier and reports the settling error. Section VI summarizes power consumption and the figure of merit. Section VII discusses the main design trade-offs. The detailed component values, transistor sizes, and simulation plots are collected in the Appendix.

II. System-Level Design

The selected ADC resolution is 9 bits and the sampling frequency is 4 MHz. The sampling period is therefore

$$T_s = \frac{1}{f_s} = \frac{1}{4\ \text{MHz}} = 250\ \text{ns}. \tag{1}$$

The nominal supply voltage is 1.8 V and the output common-mode voltage is chosen as

$$V_{CM} = 0.9\ \text{V}. \tag{2}$$

Based on the large-signal transient simulations, the differential full-scale output swing is approximately 1.8 Vpp. Since the switched-capacitor stage has a nominal gain of two, the differential full-scale input is taken as approximately 0.9 Vpp. For a 9-bit target, the LSB is

$$V_{LSB} = \frac{V_{FS}}{2^N} = \frac{0.9\ \text{V}}{512} = 1.76\ \text{mV}. \tag{3}$$

The corresponding half-LSB settling requirement is

$$\frac{V_{LSB}}{2} = 0.88\ \text{mV}. \tag{4}$$

For the switched-capacitor input stage, the sampling capacitor value is selected based on the thermal noise requirement. The sampled thermal noise is approximated by

$$V_{n,RMS}^2 = \frac{kT}{C}. \tag{5}$$

To keep the sampled noise below the required accuracy limit, the design target is chosen as

$$\frac{kT}{C} \le \frac{V_{LSB}^2}{24}. \tag{6}$$

Using $V_{LSB} = 1.76$ mV, the minimum required sampling capacitance is approximately 54 fF at room temperature. The implemented capacitor value of 800 fF is therefore sufficiently large to satisfy the thermal-noise requirement while also improving matching and reducing sensitivity to parasitics. The system-level parameters are summarized in Table I.

Maximum Tolerable Switch Resistance

Assuming an ideal OTA (infinite DC gain and bandwidth), the settling time of the switched-capacitor network is dominated by the time constant of the switch resistance and the sampling capacitor:

$$\tau = R_{sw}\, C_{samp}. \tag{7}$$

The available settling time within one clock phase is $T_{settle} = T_s/2 = 125$ ns. For 9-bit accuracy, the output must settle to within $V_{LSB}/2$ of its final value. For an exponential first-order response, this requires

$$e^{-T_{settle}/\tau} < \frac{1}{2^{N+1}}, \tag{8}$$

which gives

$$\frac{T_{settle}}{\tau} > (N+1)\ln 2 \approx 6.93. \tag{9}$$

Therefore the maximum tolerable time constant is $\tau_{max} \approx 18$ ns, and the largest tolerable switch resistance is

$$R_{sw,max} \approx \frac{\tau_{max}}{C_{samp}} = \frac{18 \text{ ns}}{800 \text{ fF}} \approx 22 \text{ k}\Omega. \tag{10}$$

The chosen transmission-gate sizes give a typical on-resistance of a few hundred Ω over the rail-to-rail input range, which is well below this limit and leaves margin for OTA-limited settling.

III. Switched-Capacitor Gain Stage

A fully differential structure is used in the switched-capacitor amplifier. Its detailed schematic is given in Fig. 6, where the two unit capacitors per side, the transmission-gate switches, and the clock phases ϕ_s and ϕ_h that control them are explicitly shown. During the sampling phase ϕ_s, the input signal is stored on the sampling capacitors. When the circuit enters the amplification phase ϕ_h, one of the capacitors is reconnected as the feedback element and the stored charge is transferred through the OTA feedback path, generating the amplified output.

Transfer Function Derivation

Consider one side of the differential circuit. Let C_1 be the input sampling capacitor and C_2 be the capacitor that becomes the feedback element in ϕ_h. Both have the same nominal value C_{samp}.

In ϕ_s, both capacitors have their left plates connected to V_{in} and their right plates connected to the OTA virtual-ground node at V_{cm}. The total charge stored on the right-plate node is

$$Q_{\phi_s} = -C_1(V_{in} - V_{cm}) - C_2(V_{in} - V_{cm}). \tag{11}$$

In ϕ_h, the left plate of C_1 is reconnected to V_{cm} (since the gain-of-two configuration corresponds to $X = 0$, so the reference is not applied) and the left plate of C_2 is reconnected to V_{out}. The OTA virtual-ground node remains at V_{cm}. The new total charge is

$$Q_{\phi_h} = -C_1(V_{cm} - V_{cm}) - C_2(V_{out} - V_{cm}). \tag{12}$$

Since the OTA input node is high-impedance, charge is conserved between the two phases:

$$(C_1 + C_2)(V_{in} - V_{cm}) = C_2(V_{out} - V_{cm}). \tag{13}$$

With $C_1 = C_2 = C_{samp}$, this simplifies to

$$V_{out} - V_{cm} = 2(V_{in} - V_{cm}), \tag{14}$$

and, by applying the same analysis to both sides of the fully differential circuit, the differential output is

$$V_{out,diff} = 2\, V_{in,diff}. \tag{15}$$

Switch Sizing and Charge Injection

The unit capacitor value is chosen as 800 fF. Each transmission gate consists of a 2.5 µm / 180 nm NMOS transistor together with a 5 µm / 180 nm PMOS transistor (see Fig. 4). A larger PMOS width is used because hole mobility is lower than electron mobility, which helps keep the switch resistance more uniform across the input range. Using both NMOS and PMOS devices also improves linearity and reduces distortion compared with a single NMOS switch.

Charge injection from the switches is another important non-ideality. When a MOS switch turns off, the channel charge $Q_{ch} \approx WLC_{ox}(V_{GS} - V_{TH})$ is partly injected onto the sampling capacitor and causes an offset and signal-dependent error. The transmission-gate structure in Fig. 4, where the NMOS and PMOS devices are driven by complementary clocks, reduces this effect because the two channel charges have opposite signs and partially cancel. The fully differential topology further suppresses the common-mode component of the residual injection. Bottom-plate sampling, achieved by opening the OTA-side switches slightly earlier than the input-side switches in the non-overlapping clock scheme, helps fix the injected charge to a signal-independent value so that only a small common-mode offset remains after differential combination.

IV. OTA and Common-Mode Feedback Design

Topology Selection

The OTA uses a fully differential two-stage architecture with Miller compensation. The detailed transistor-level schematic is shown in Fig. 2, where the PMOS differential input pair, the cascoded PMOS active loads, the NMOS current-sink devices of the first stage, the common-source output transistors of the second stage, and the Miller compensation capacitors C_C with their series damping resistors R_Z between the two stages can all be identified. The first stage gives high DC gain, the second stage gives a large output swing, and the Miller compensation produces a well-controlled dominant pole and adequate phase margin.

A telescopic cascode topology was also considered, but it has a smaller output swing because two extra cascode transistors stack between the supply rails. For a 1.8 V supply with $V_{CM} = 0.9$ V and a target differential full-scale swing of 1.8 Vpp, the telescopic topology leaves very little headroom. A folded-cascode topology gives a larger swing but typically

achieves a smaller DC gain than a two-stage design, which would make the static gain error harder to control for a 9-bit target. The two-stage Miller-compensated OTA was therefore selected as the best compromise between gain, output swing, and power for this design.

PMOS input devices are used to make the input common-mode range compatible with $V_{CM} = 0.9$ V and to reduce the flicker noise contribution from the input pair. Cascoding is included in the first stage to raise the output resistance and increase the overall DC gain. All transistor sizes are listed in Table III.

OTA Specification Derivation

The OTA specifications are derived from the settling-accuracy requirement of the switched-capacitor stage. Since $C_1 = C_2 = C_{samp}$, the feedback factor of the closed-loop amplifier is

$$\beta = \frac{C_2}{C_1 + C_2} = \frac{1}{2}, \tag{16}$$

neglecting parasitics. The closed-loop static gain error caused by finite OTA DC gain A_0 is approximately

$$\epsilon_{gain} \approx \frac{1}{A_0 \beta}. \tag{17}$$

For the error to remain smaller than $V_{LSB}/V_{FS} = 1/2^N$ at the output, the minimum DC gain is

$$A_{0,min} \approx \frac{2^N}{\beta} = 2^{N+1} \approx 1024 \ \ (60 \text{ dB}). \tag{18}$$

The settling speed is set by the closed-loop bandwidth $\text{BW}_{cl} = \beta \cdot \text{GBW}$. For first-order exponential settling to within $V_{LSB}/2$ in the available time $T_{settle} = T_s/2 = 125$ ns, we need

$$\text{GBW}_{min} = \frac{(N+1)\ln 2}{2\pi\beta\, T_{settle}} \approx 17.6 \text{ MHz}. \tag{19}$$

A phase margin of at least 60° is required to avoid significant ringing during large-signal transitions. A slew rate large enough to traverse the full-scale differential swing in a small fraction of T_{settle} is also required; using SR $\geq V_{FS}/(T_{settle}/4) \approx 30$ V/µs as a guideline.

The OTA was characterized using the AC testbench shown in Fig. 7, which applies a small differential AC excitation around $V_{CM} = 0.9$ V and reads the differential output through an ideal common-mode rejecting probe. The resulting magnitude and phase curves are plotted in Fig. 7: the low-frequency magnitude reads about 90.86 dB, the magnitude curve crosses 0 dB at 47.86 MHz, and the phase at this crossover frequency is 99.68°, giving a phase margin of 80.32°. All of these values are well above the analytical minimums derived earlier, leaving comfortable margin for parasitic loading, process variation, and large-signal slewing. The OTA performance is summarized in Table IV.

Noise Budget

The sampled thermal noise of one switch–capacitor branch is

$$V_{n,sw}^2 = \frac{kT}{C_{samp}} \approx 5.2 \times 10^{-9} \text{ V}^2, \tag{20}$$

which corresponds to a noise voltage of about 72 µV RMS at $C_{samp} = 800$ fF. To prevent the OTA from dominating the total noise, the input-referred OTA noise integrated over the closed-loop bandwidth is targeted to be of the same order of magnitude as the switch noise. Schematic-level estimation using g_m of the input pair and $g_m/g_{m,load}$ ratio of the active loads gives an input-referred noise on the order of 50–100 µV RMS over the closed-loop bandwidth, which satisfies the requirement that the input-referred OTA noise and the sampled switch noise are of similar order.

Common-Mode Feedback

A common-mode feedback loop is required, since the differential signal path alone does not define the output common-mode voltage in a fully differential amplifier. A switched-capacitor CMFB scheme is adopted, with the detailed schematic shown in Fig. 3. The two sense capacitors take the average of the two output nodes and refresh against the $V_{cm} = 0.9$ V reference each cycle, and the resulting control voltage V_{CMFB} adjusts the load-side bias of the OTA so that the output common-mode level is held at 0.9 V.

The CMFB loop must have sufficient bandwidth and phase margin so that the common-mode voltage tracks any disturbance fast enough during normal switched-capacitor operation. The common-mode AC response in Fig. 8 shows that the common-mode loop has a comparable unity-gain bandwidth to the differential path and a phase margin well above 60°. The standalone common-mode step response in Fig. 9 further confirms this: after a small disturbance the output common-mode level returns to the 0.9 V reference within one sampling period and does not show under-damped ringing. Therefore the common-mode loop does not limit the overall settling.

V. Transient Verification of the Complete Design

The full switched-capacitor amplifier was verified with transient simulations using the testbench shown in Fig. 10, where the differential input source, the non-overlapping clock generator, and the load capacitor that emulates the next pipeline stage can be identified. A 250 ns clock period was used, corresponding to the 4 MHz sampling rate.

Clock Generation

The two clock phases ϕ_s and ϕ_h are generated by vpulse sources from analogLib and combined into a non-overlapping pair similar to the cross-coupled NAND structure described in Johns and Martin Fig. 14.3. A non-overlap dead time of a few nanoseconds is inserted between the two phases to make sure that both ϕ_s and ϕ_h are never high at the same time, which prevents direct charge sharing between the input and the OTA output node during the transition. The OTA-side input switches

are turned off slightly before the input-side switches (bottom-plate sampling) so that the channel charge that is injected onto the sampling capacitor becomes independent of the input signal and only produces a small common-mode offset that is rejected by the differential structure.

Small-Signal Gain Verification

Small-signal behavior was verified with differential input amplitudes of 5 mV and 10 mV. Fig. 11 shows the 5 mV case, where the output reaches a flat hold level of about 10.005 mV during each ϕ_h interval. Fig. 12 shows the 10 mV case, where the hold level reaches about 20.010 mV. Both correspond to a closed-loop gain of 2.001 and a gain error well below $V_{LSB}/V_{FS} \approx 0.2\%$. The flatness of the hold portion in both figures indicates a small-signal settling error on the order of 5 µV, which is far smaller than $V_{LSB}/2 = 0.88$ mV, so the small-signal accuracy requirement is met with large margin.

In the small-signal step-response test (Fig. 13), the differential input changes from $+V_{LSB}$ to $-V_{LSB}$ and then returns to $+V_{LSB}$. The output waveform in the figure tracks the expected $\pm 2V_{LSB}$ levels within one sampling period at each transition and the settled error in the hold portion stays inside $V_{LSB}/2$. This confirms that the amplifier can settle correctly for the smallest step size relevant to the 9-bit ADC resolution.

A close inspection of the hold portion of Fig. 12 also reveals a slow tilt of approximately 75 µV across one hold interval. This droop is mainly caused by leakage on the OTA output node and by sub-threshold conduction of the off-state switches across the hold capacitor. Since 75 µV is much smaller than $V_{LSB}/2$, this droop does not affect the 9-bit accuracy target.

Ramp Test

For the ramp test, the required ramp period is

$$T_{ramp} = \frac{1}{20 f_s} = \frac{1}{20 \times 4\ \text{MHz}} = 12.5\ \text{ns}, \tag{21}$$

This follows the project-specified ramp-period requirement. The differential ramp input covers the full-scale range $[-V_{FS}, +V_{FS}]$. The simulated output in Fig. 14 reproduces the input ramp at twice the slope, and the staircase shape of the output reflects the sample-and-hold operation: the output stays flat during ϕ_h and jumps to the next level at the start of each ϕ_h. No clipping or instability is observed even at the two extreme ends of the ramp, which shows that the closed-loop circuit remains in its linear operating region across the full input range.

Large-Signal Step Response

The large-signal step-response result is shown in Fig. 15, where the input switches from $+V_{FS}$ to $-V_{FS}$ and then returns to $+V_{FS}$. At the beginning of each hold phase a transient overshoot can be seen at the peak of the differential output, and the waveform then settles to a lower steady level. The differential output reaches a maximum value of about 909.6 mV before settling near 843.0 mV. A short negative glitch of roughly -6.1 mV can also be observed near each clock transition in the same figure. The overshoot is estimated as

$$\text{Overshoot} = \frac{0.9096 - 0.8430}{0.8430} \times 100\% \approx 7.9\%. \tag{22}$$

The observed overshoot is mainly caused by the finite phase margin and the high-speed closed-loop transient behavior of the OTA under large-signal switching, where the OTA briefly enters the slewing region before recovering to linear settling. The short negative glitch visible at each clock edge in Fig. 15 is caused by clock feedthrough and charge injection from the input-side and feedback-side switches as they turn on at the beginning of the hold phase; this glitch is much shorter than the settling time and disappears before the end of the hold phase. Although transient ringing appears during the clock transition, the output still settles to its final value before the next sampling phase begins.

At full scale, the output settled value of 0.843 V is close to but not exactly 0.9 V because the OTA output stage starts to approach the supply rail and lose some linearity at the largest differential swing. For inputs that are slightly inside the nominal full-scale range, the gain error drops back to the small-signal value and the settling error stays within $V_{LSB}/2 = 0.88$ mV. The complete set of transient measurements extracted from Figs. 11–15 is summarized in Table V.

VI. Power Consumption and Figure of Merit

The measured average supply current of the complete switched-capacitor amplifier is approximately 250 µA. Therefore, the total power consumption is

$$P_{total} = V_{DD}\, I_{avg} = 1.8\ \text{V} \times 250\ \mu\text{A} = 450\ \mu\text{W}. \tag{23}$$

The current consumption is dominated by the OTA core, which draws about 100 µA (180 µW). The bias-generation circuit and the common-mode feedback network together consume on the order of 100 µA, mainly because the CMFB branch must keep its own bias devices in saturation and provide enough loop bandwidth to track the differential output transients. The remaining current is associated with the switched-capacitor dynamic power, including the energy used each cycle to charge and discharge the sampling and feedback capacitors through the transmission-gate switches. The detailed power breakdown is listed in Table VI.

The project figure of merit is defined as

$$\text{FOM} = \frac{P}{2^{ENOB}\, f_s}. \tag{24}$$

Using $P = 450$ µW, $ENOB = 9$, and $f_s = 4$ MHz,

$$\text{FOM} = \frac{450\ \mu\text{W}}{2^9 \times 4\ \text{MHz}} = 0.220\ \text{pJ/conv.-step}. \tag{25}$$

Following the project specification, the nominal resolution $N = 9$ is used directly as the ENOB in the FOM calculation.

VII. Design Discussion

The design is constrained by trade-offs among settling speed, power consumption, capacitor size, and switch non-idealities. A higher OTA bias current improves bandwidth and settling but increases power consumption. Larger capacitors reduce thermal noise and improve matching, although they also increase the OTA load and area. The selected 800 fF unit capacitor provides a compromise between noise, settling performance, and implementation cost.

Simulation results show stable switched-capacitor operation under both small-signal and full-scale differential inputs. Although large-signal transitions produce some overshoot, the output settles to the correct steady-state value within the available clock period.

The OTA gain-bandwidth product and phase margin are sufficient for stable closed-loop operation at the target frequency, while the CMFB circuit maintains proper output common-mode regulation.

Further improvement of the transient response would likely require either a higher OTA bias current or additional compensation optimization. Increasing the bias current would improve settling speed at the cost of more power, while stronger compensation would reduce overshoot at the cost of bandwidth and settling speed. The final design therefore represents a compromise among gain, bandwidth, phase margin, settling accuracy, and power efficiency.

Ramp-input simulations show that the circuit remains stable across the full differential input range. No output clipping or instability is observed within the intended operating region.

VIII. Conclusion

A fully differential switched-capacitor amplifier for a pipelined ADC residue stage was designed and verified through schematic-level Spectre simulations. The complete circuit topology is given in Fig. 1 and 5, with the transistor-level OTA in Fig. 2 and the switched-capacitor CMFB network in Fig. 3. The circuit achieves the intended closed-loop gain of two while supporting 4 MHz sampling operation with a 9-bit target resolution.

The differential AC response in Fig. 7 together with the common-mode results in Figs. 8 and 9 show that the OTA provides sufficient gain, bandwidth, and phase margin for reliable closed-loop operation at the target sampling frequency. The transient verification in Figs. 11–15 confirms accurate small-signal settling, stable behavior across the full-scale ramp, and well-controlled overshoot for full-scale step inputs.

The complete amplifier consumes about 450 μW from a 1.8 V supply, giving a figure of merit of approximately 0.220 pJ/conversion-step. The overall performance summary in Tables I–VI shows that, based on the schematic-level results, the design meets the main project requirements for gain accuracy, settling performance, stability, and power consumption.

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APPENDIX

TABLES

TABLE I
SYSTEM-LEVEL AND PERFORMANCE SUMMARY

Parameter	Value
Technology	180 nm CMOS (TSMC018)
Process corner	TT
Temperature	300 K
Supply voltage	1.8 V
Common-mode voltage	0.9 V
Sampling frequency	4 MHz
Sampling period	250 ns
Resolution target	9 bits
Differential full-scale input	0.9 Vpp
Differential full-scale output	1.8 Vpp
LSB size	1.76 mV
Half-LSB target	0.88 mV
Nominal gain	2

TABLE II
PASSIVE COMPONENT AND SWITCH SUMMARY

Component	Value	Function
C0–C3	800 fF each	SC unit capacitors
C22, C23	560.6 fF	OTA Miller compensation capacitors
R0, R1	2 kΩ	Compensation damping resistors
R2, R3	1.6 MΩ	Output common-mode sensing resistors
sw_np NMOS	2.5 µm / 180 nm	Transmission-gate NMOS
sw_np PMOS	5 µm / 180 nm	Transmission-gate PMOS

TABLE III
OTA AND CMFB TRANSISTOR SIZING SUMMARY

Devices	Type	W/L	Function
M0, M13	PMOS	10 µm / 0.5 µm	Differential input pair
M47, M48	PMOS	10 µm / 0.5 µm	Input branch cascode devices
M49–M52	PMOS	10 µm / 0.5 µm	PMOS cascoded loads
M55–M58	PMOS	10 µm / 0.5 µm	Output branch PMOS loads
M1, M2, M4–M7	PMOS	10 µm / 0.5 µm	PMOS bias mirrors
M3	PMOS	1 µm / 0.5 µm	PMOS bias reference
M24, M25	NMOS	5 µm / 0.5 µm	NMOS current sink devices
M10, M11	NMOS	5 µm / 0.5 µm	NMOS bias devices
M53, M54	NMOS	5 µm / 1 µm	CMFB-controlled sink devices
M14, M15	NMOS	5 µm / 1 µm	CMFB current source devices
M8	NMOS	1 µm / 2 µm	NMOS bias reference
M9, M16	NMOS	10 µm / 0.18 µm	Output pull-down devices
M38, M39	PMOS	10 µm / 0.5 µm	CMFB control devices
M59, M60	PMOS	10 µm / 0.5 µm	CMFB PMOS load devices

TABLE IV
OTA AC PERFORMANCE SUMMARY

Parameter	Value
DC gain	90.86 dB
Unity-gain bandwidth	47.86 MHz
Phase margin	80.32°
OTA average current	100 µA
OTA core power	180 µW

TABLE V
OVERALL TRANSIENT VERIFICATION SUMMARY

Test Case	Measured Result	Comment
5 mV input	10.005 mV output	Gain close to 2
10 mV input	20.010 mV output	Gain close to 2
Small step	See Fig. 13	V_{LSB} step verification
Ramp input	See Fig. 14	Full-scale ramp verification
Large-signal peak	909.6 mV	Full-scale transient swing
Large-signal settled	843.0 mV	Settled hold value
Negative glitch	-6.1 mV	Clock transition artifact
Overshoot	7.9%	Stable response
Hold droop	≈ 75 µV	Small-signal hold case

TABLE VI
POWER AND FOM SUMMARY

Parameter	Value
OTA core current	100 µA
OTA core power	180 µW
Total average supply current	250 µA
Total power	450 µW
ENOB used for FOM	9 bits
Sampling frequency	4 MHz
FOM	0.220 pJ/conversion-step

FIGURES

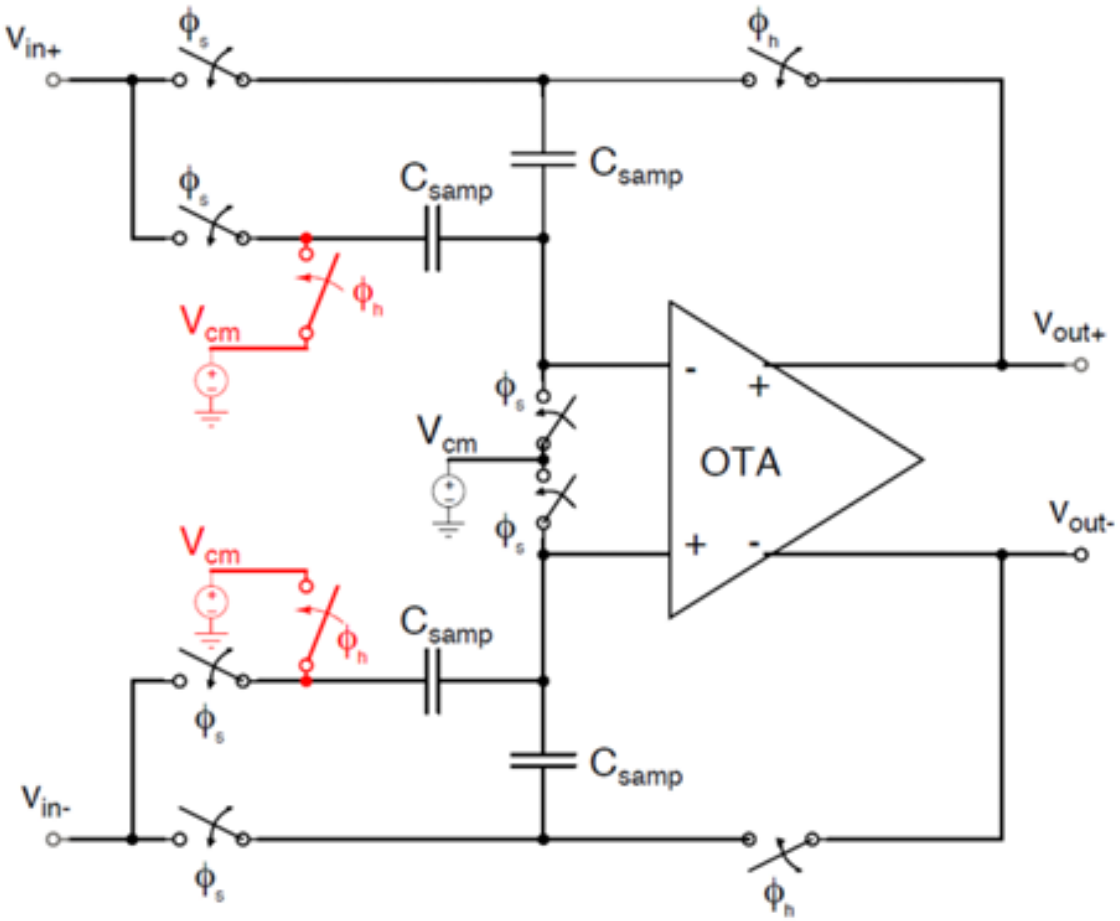


Fig. 1. Overall schematic of the fully differential switched-capacitor sample-and-hold amplifier including OTA, CMFB, transmission-gate switches, and sampling capacitors.

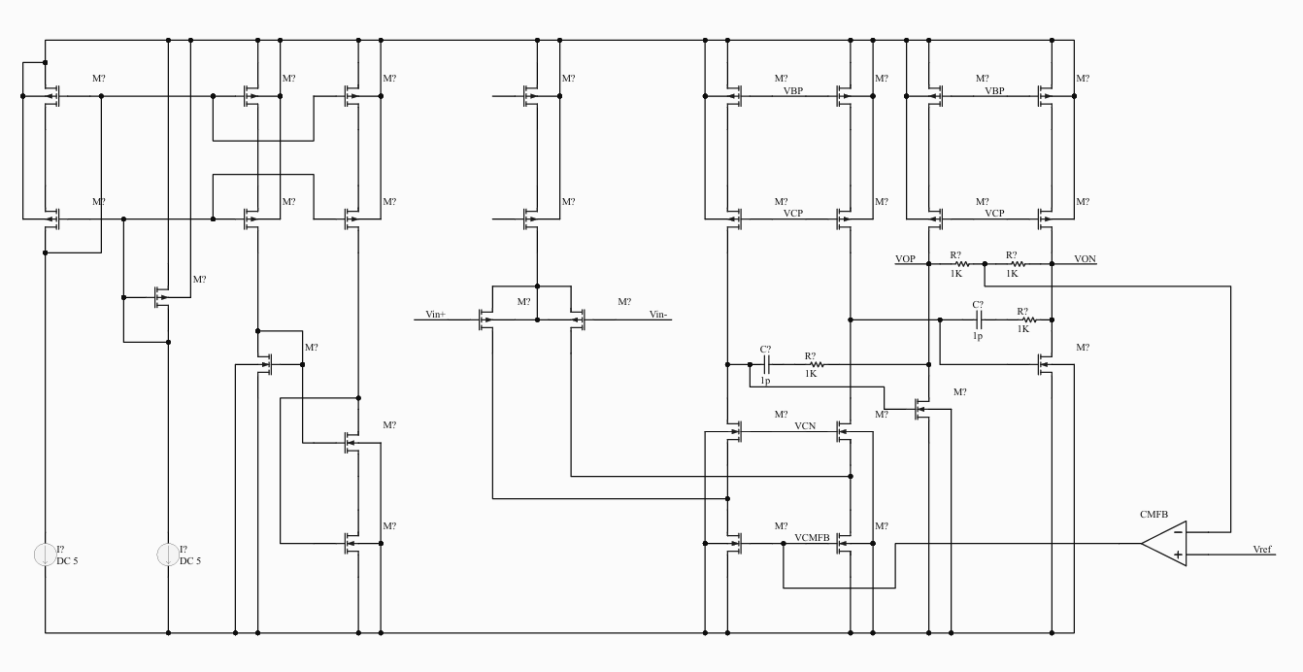


Fig. 2. Transistor-level schematic of the fully differential OTA used in the switched-capacitor gain stage. The amplifier uses a PMOS differential input pair together with cascoded PMOS active loads and NMOS current-sink devices to achieve high output resistance, large DC gain, and stable differential amplification.

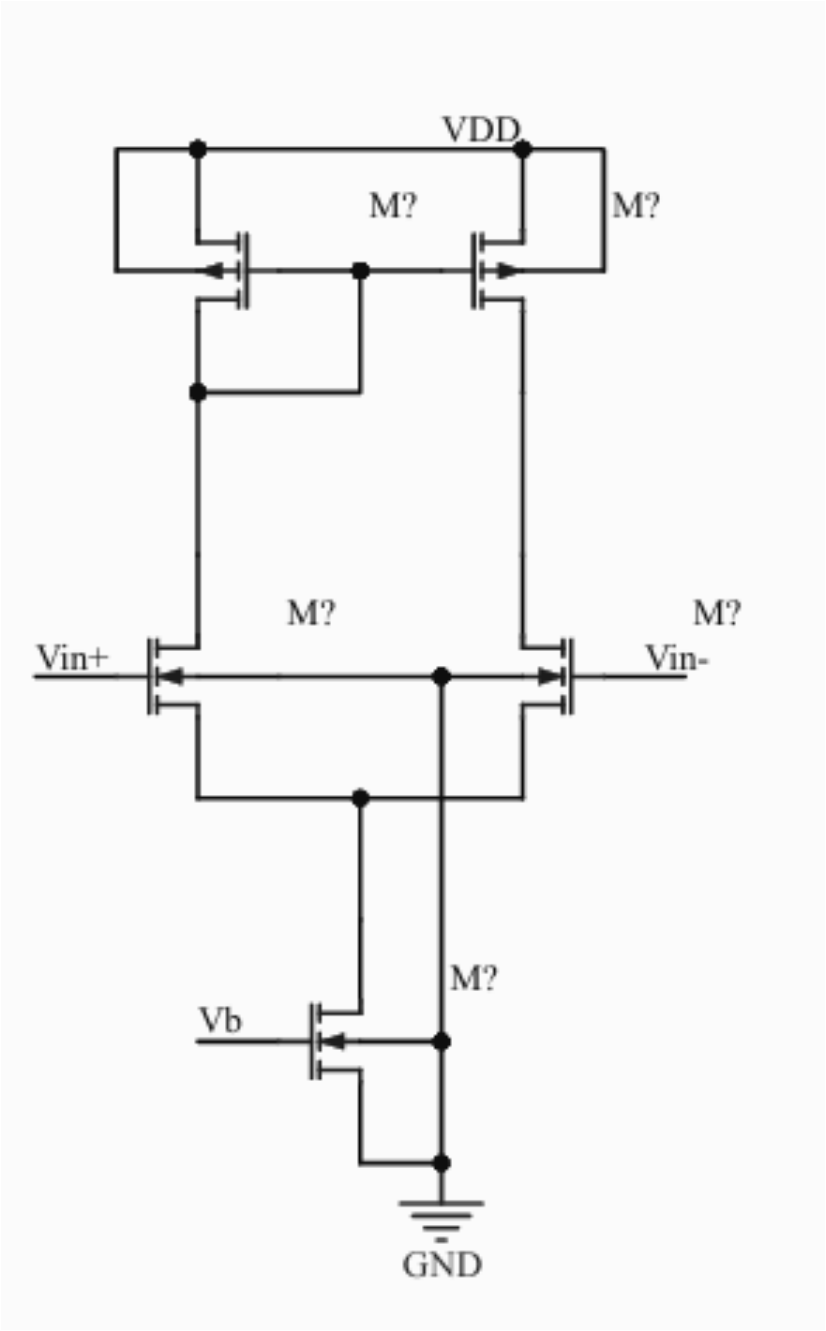


Fig. 3. Transistor-level common-mode feedback (CMFB) amplifier used to regulate the OTA output common-mode voltage. The circuit senses the differential output common-mode level and generates the control voltage V_{CMFB} used to bias the OTA current-source devices and stabilize the output common-mode voltage near 0.9 V.

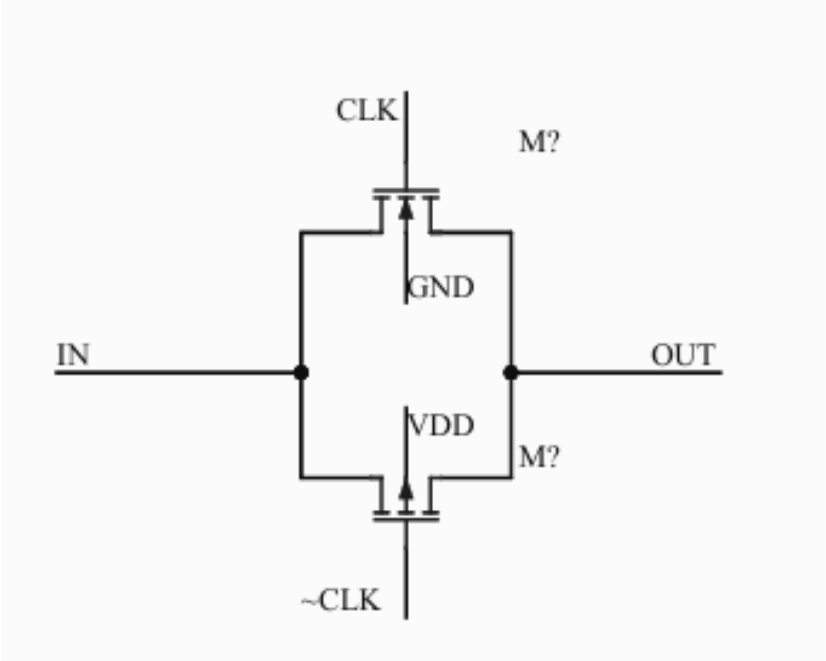


Fig. 4. Transmission-gate switch schematic used in the switched-capacitor circuit. NMOS and PMOS devices are controlled by complementary clock signals to achieve a wide rail-to-rail input range and reduced charge-injection imbalance.

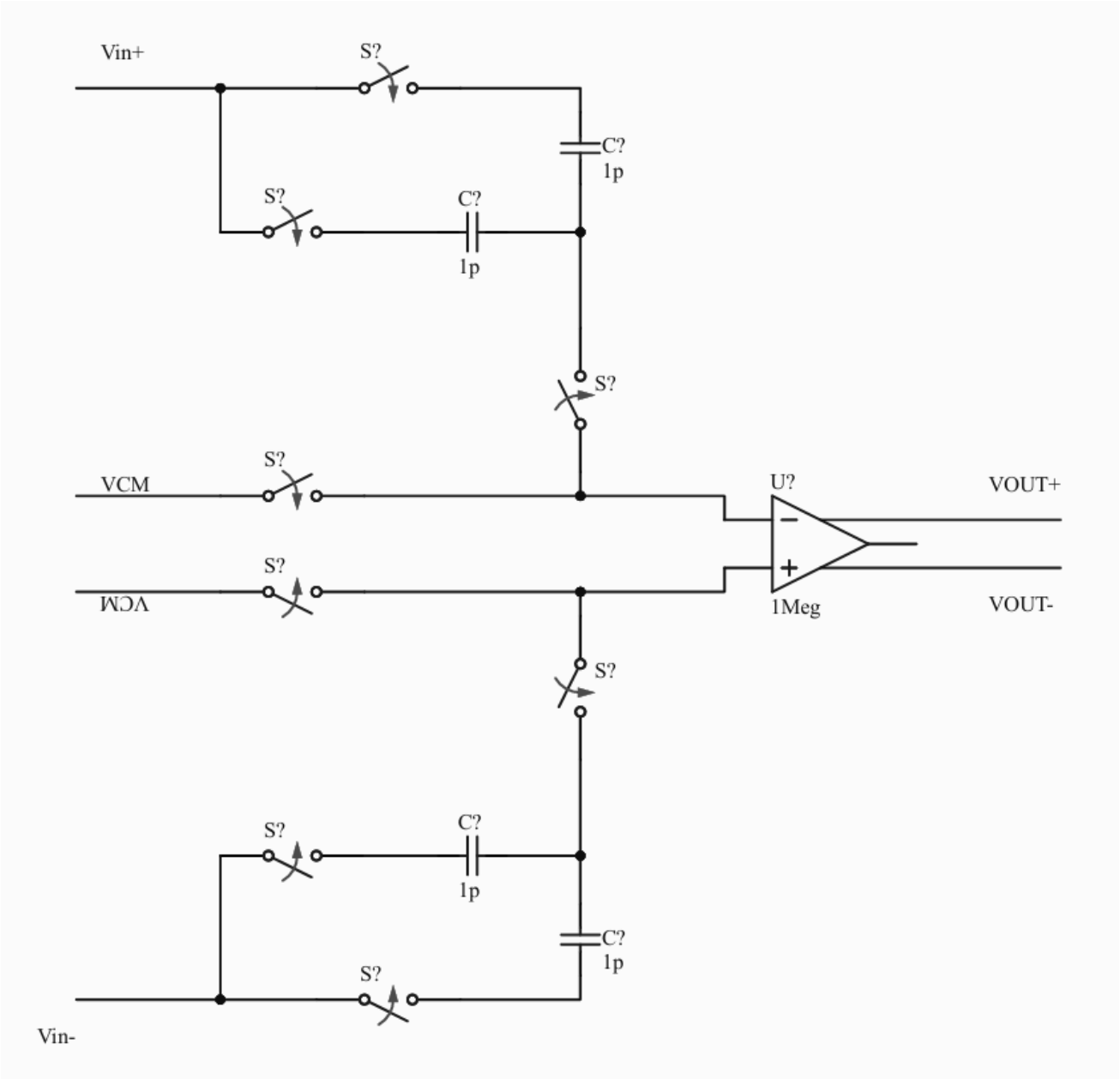


Fig. 5. Switched-capacitor gain-of-two amplifier schematic. The design includes MOS transmission-gate switches, sampling capacitors, feedback capacitors, non-overlapping clock phases, and the fully differential OTA to implement charge-domain amplification with a nominal gain of two.

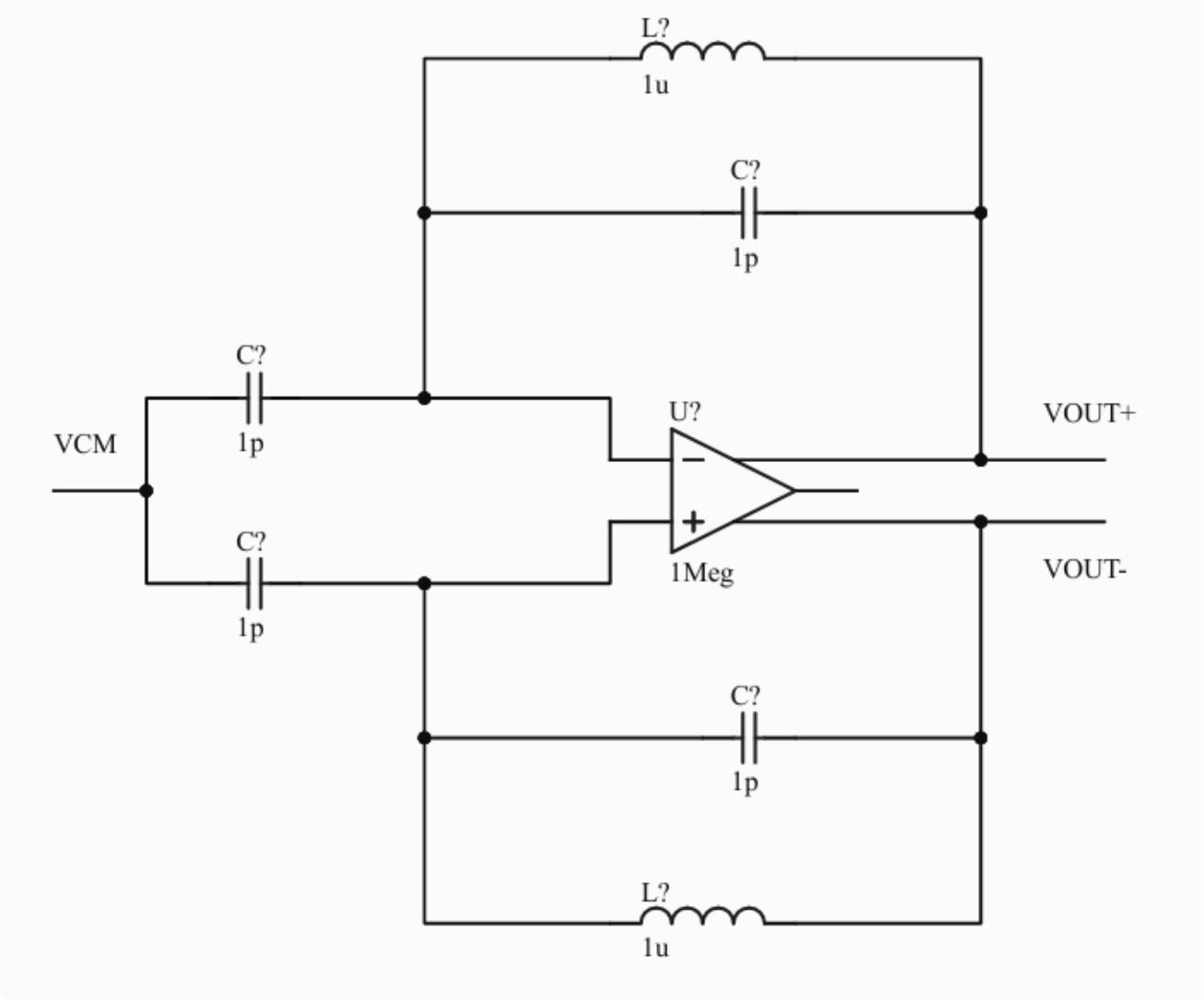


Fig. 6. AC simulation testbench used to characterize the differential frequency response of the OTA. The setup applies differential AC excitation around the desired common-mode voltage and is used to extract the DC gain, unity-gain bandwidth, and phase margin required for closed-loop stability verification.

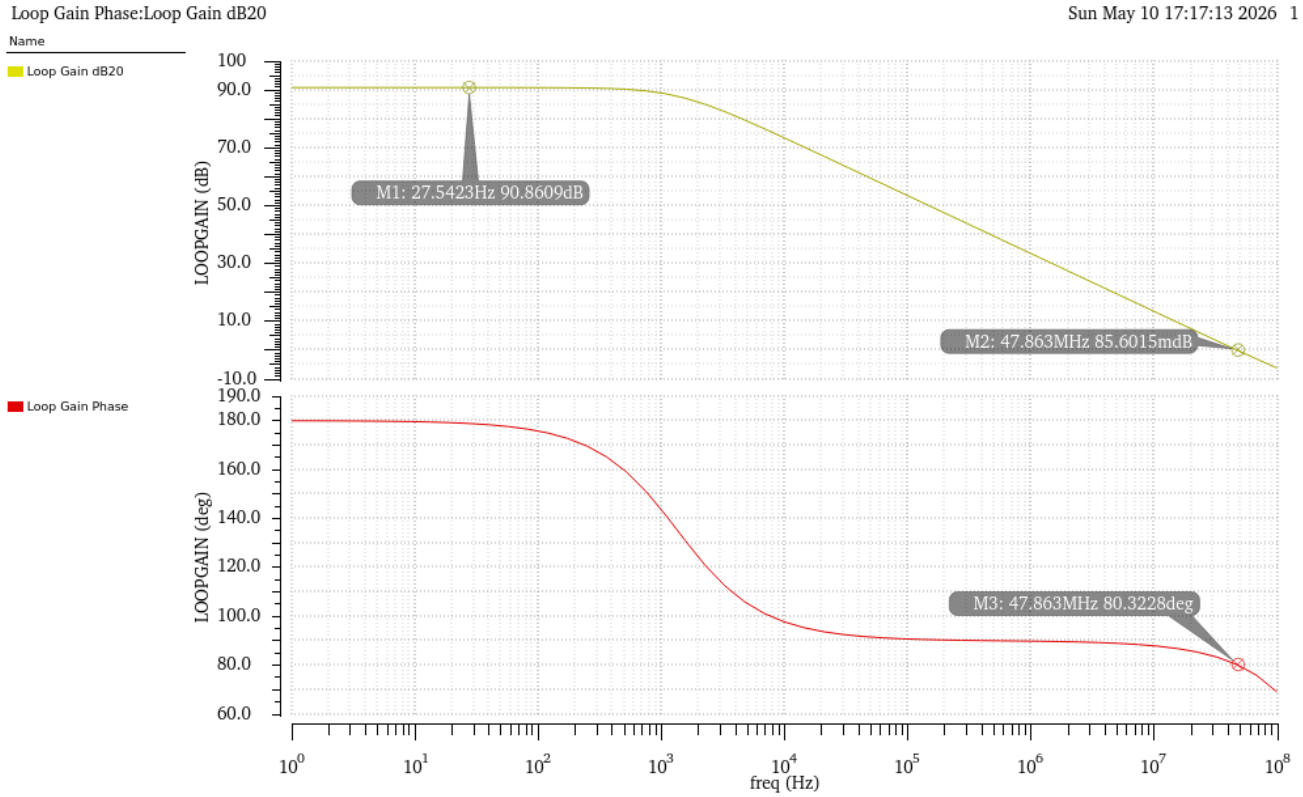


Fig. 7. Differential AC response of the OTA showing 90.86 dB DC gain, 47.86 MHz unity-gain bandwidth, and 80.32° phase margin for stable closed-loop switched-capacitor operation.

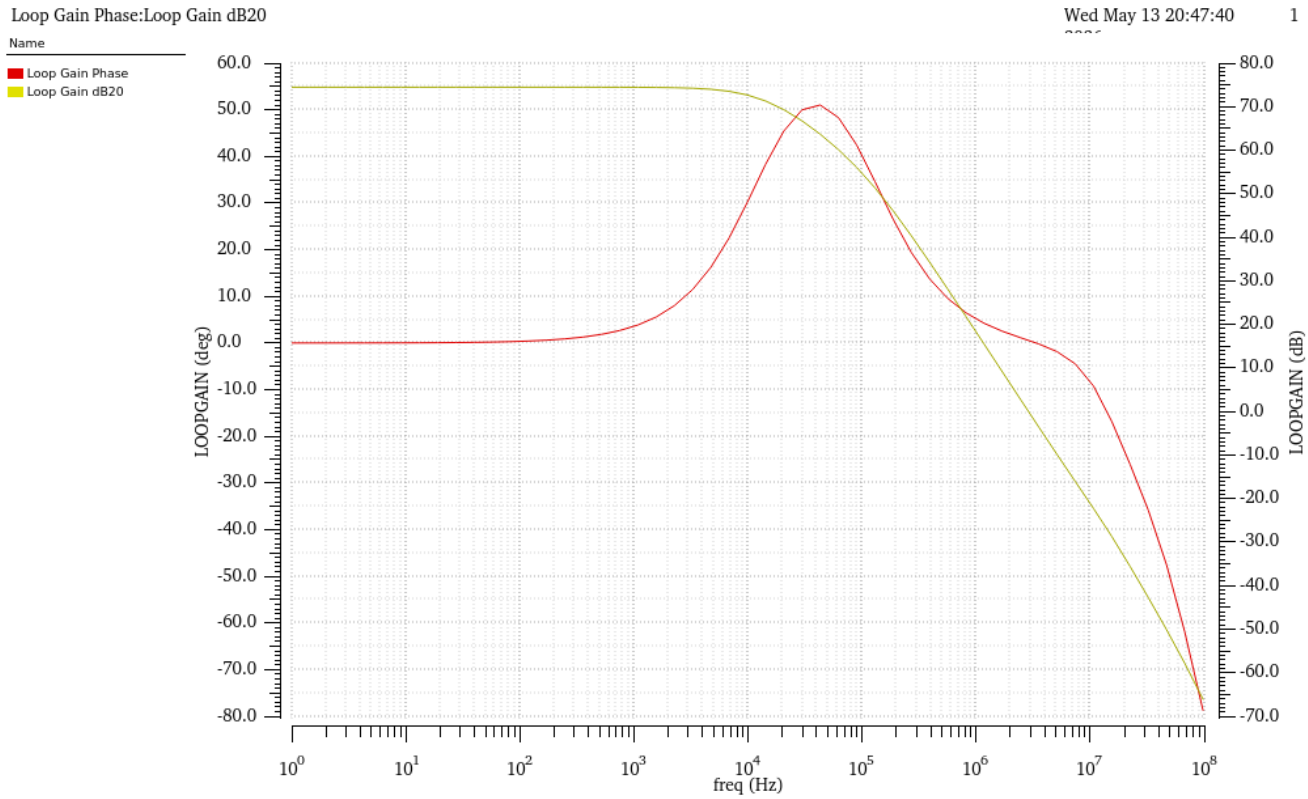


Fig. 8. Common-mode AC response of the OTA used to verify the stability and bandwidth of the common-mode feedback loop under common-mode excitation.

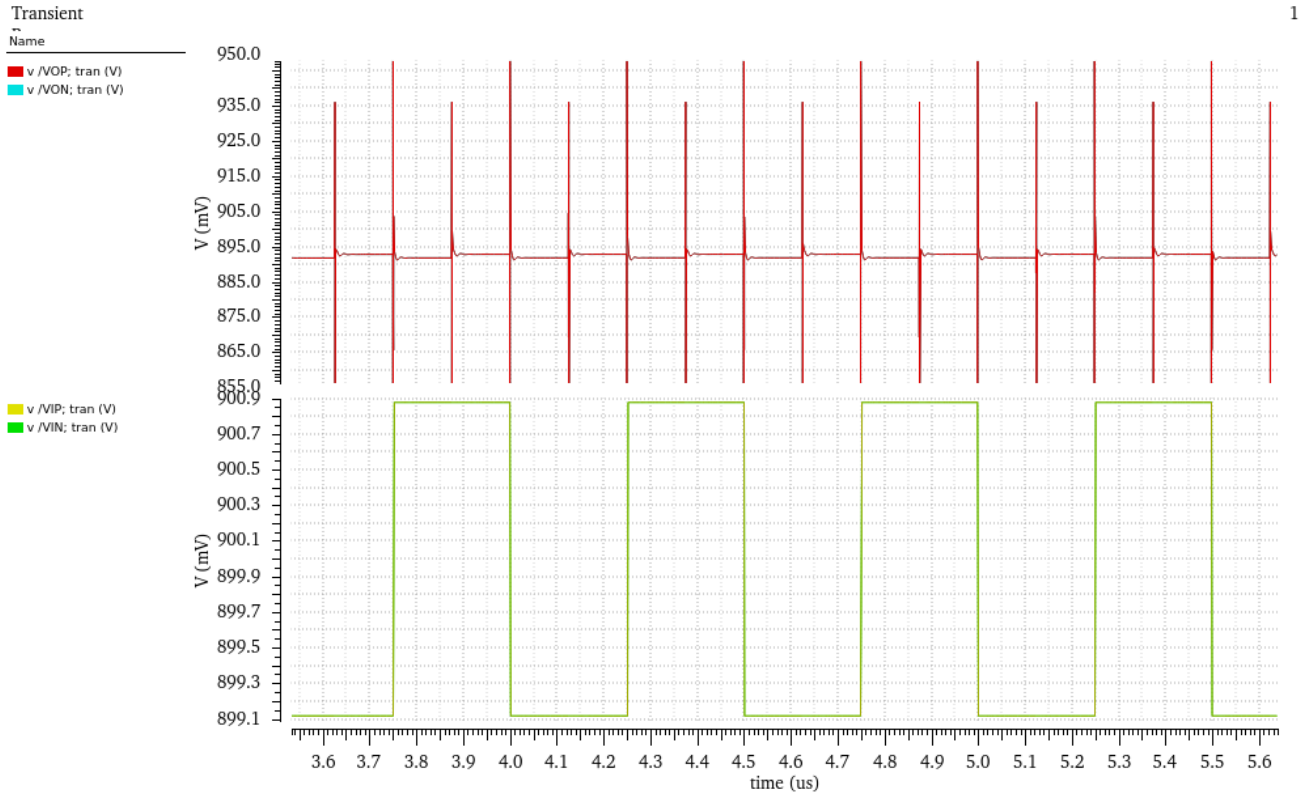


Fig. 9. Standalone OTA common-mode transient response showing regulation of the output common-mode voltage around the target value of 0.9 V during transient operation.

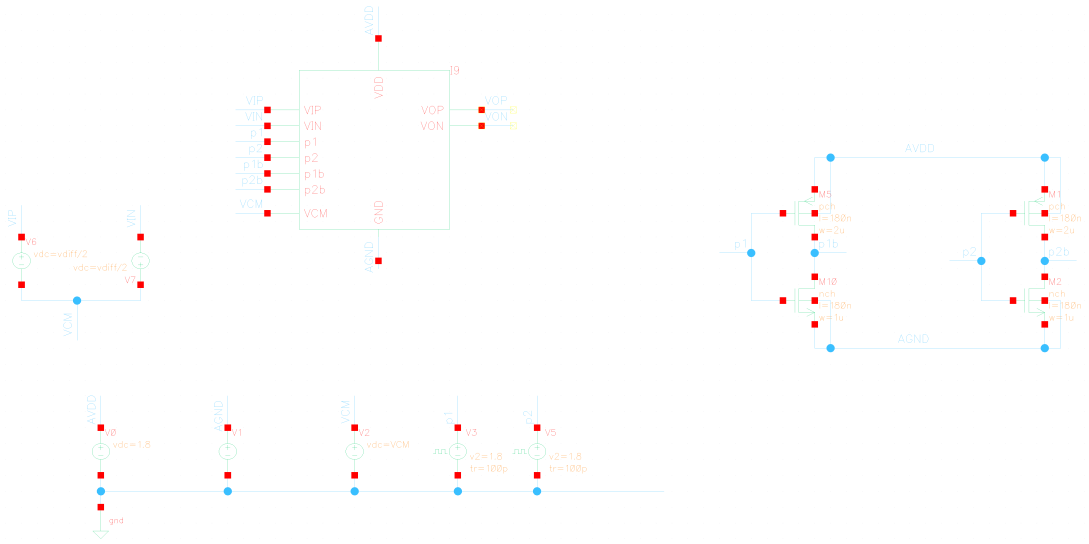


Fig. 10. Transient simulation testbench for the complete switched-capacitor amplifier including the OTA, switched capacitors, non-overlapping clock phases, differential input sources, and clock control signals. The setup is used to evaluate gain accuracy, settling behavior, ramp response, and large-signal transient operation of the complete switched-capacitor stage. Due to the complexity and simulator-specific nature of the transient verification setup, the original Cadence schematic view is shown directly for clarity.

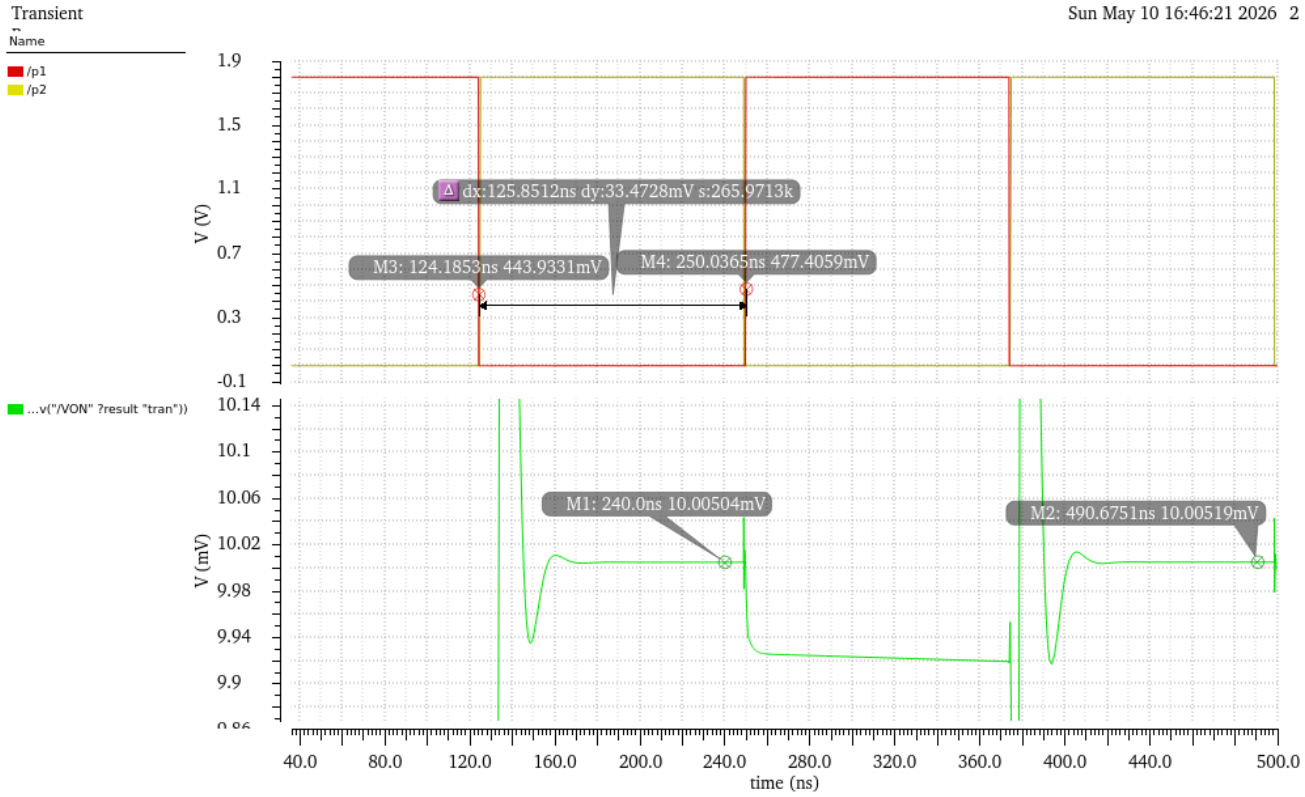


Fig. 11. Transient response of the complete switched-capacitor amplifier for a 5 mV differential input signal, demonstrating approximately 2× closed-loop gain together with stable settling behavior.

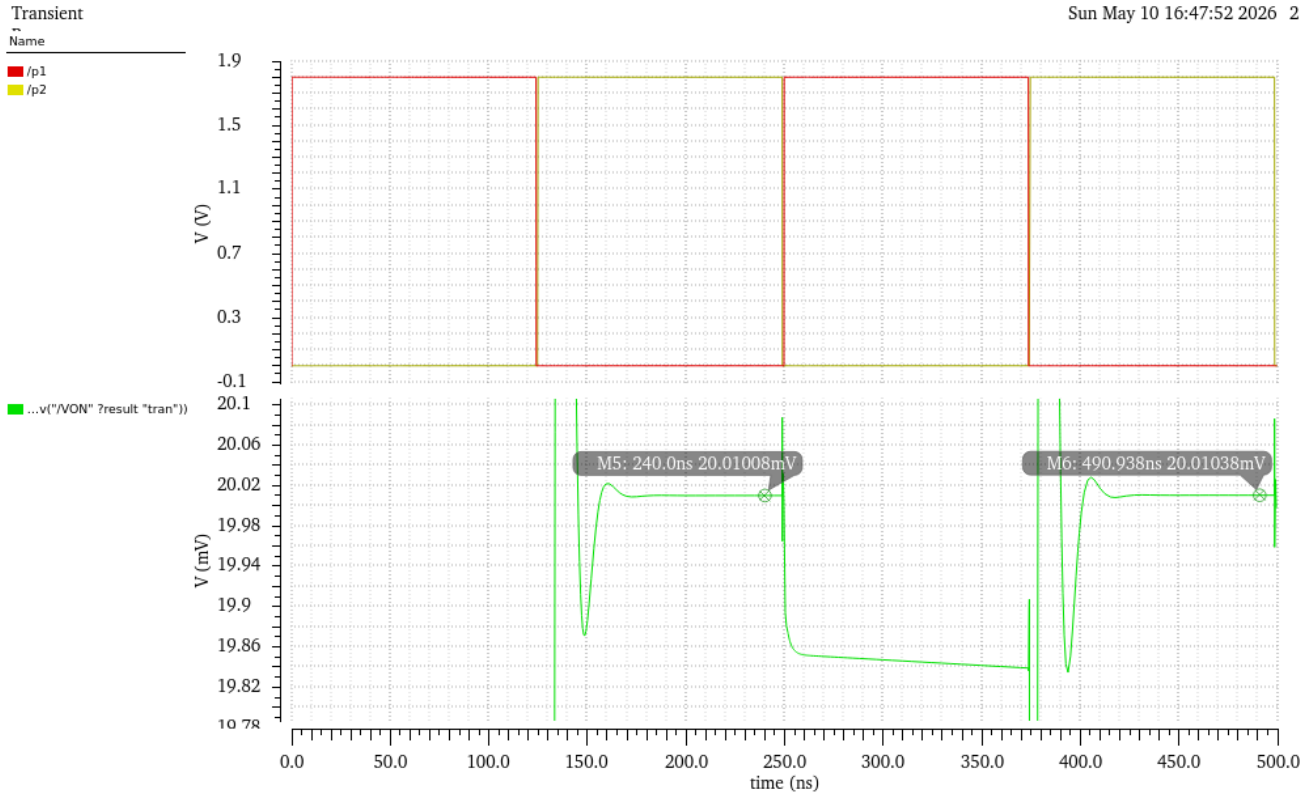


Fig. 12. Transient response of the complete switched-capacitor amplifier for a 10 mV differential input signal, confirming accurate gain-of-two amplification and stable transient operation.

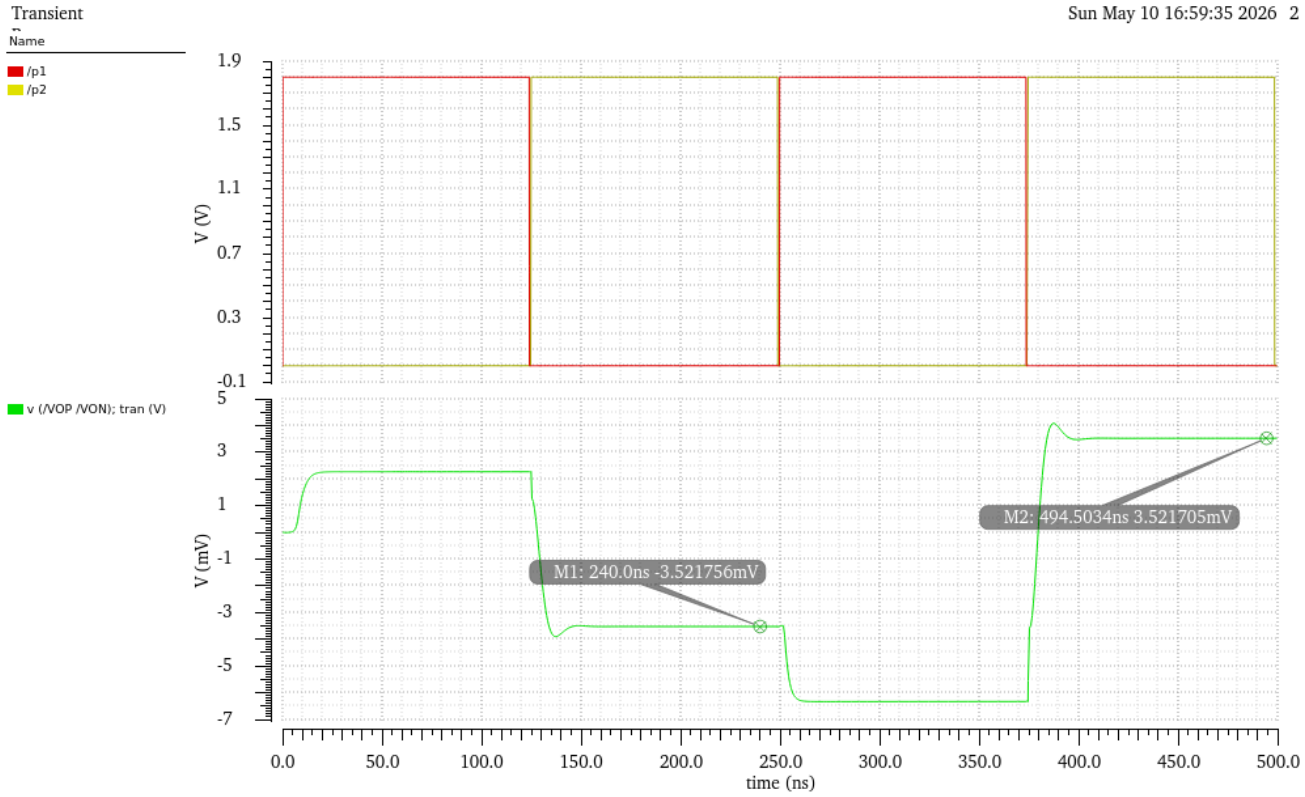


Fig. 13. Small-signal transient response of the complete switched-capacitor amplifier for an input transition from $+V_{LSB}$ to $-V_{LSB}$ and back to $+V_{LSB}$, verifying settling performance near the ADC resolution limit.

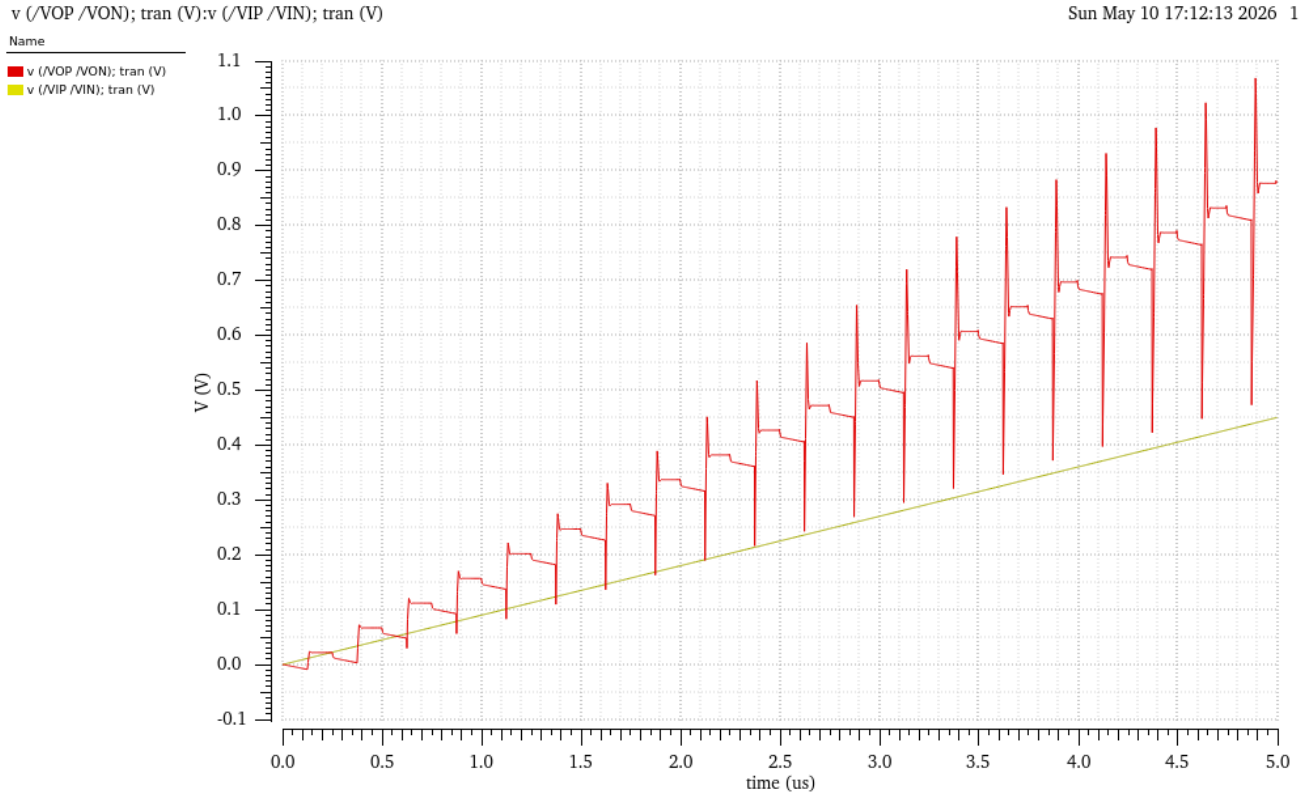


Fig. 14. Ramp-input transient response of the complete switched-capacitor amplifier for a full-scale differential ramp input covering the full range, demonstrating stable operation across the intended input range.

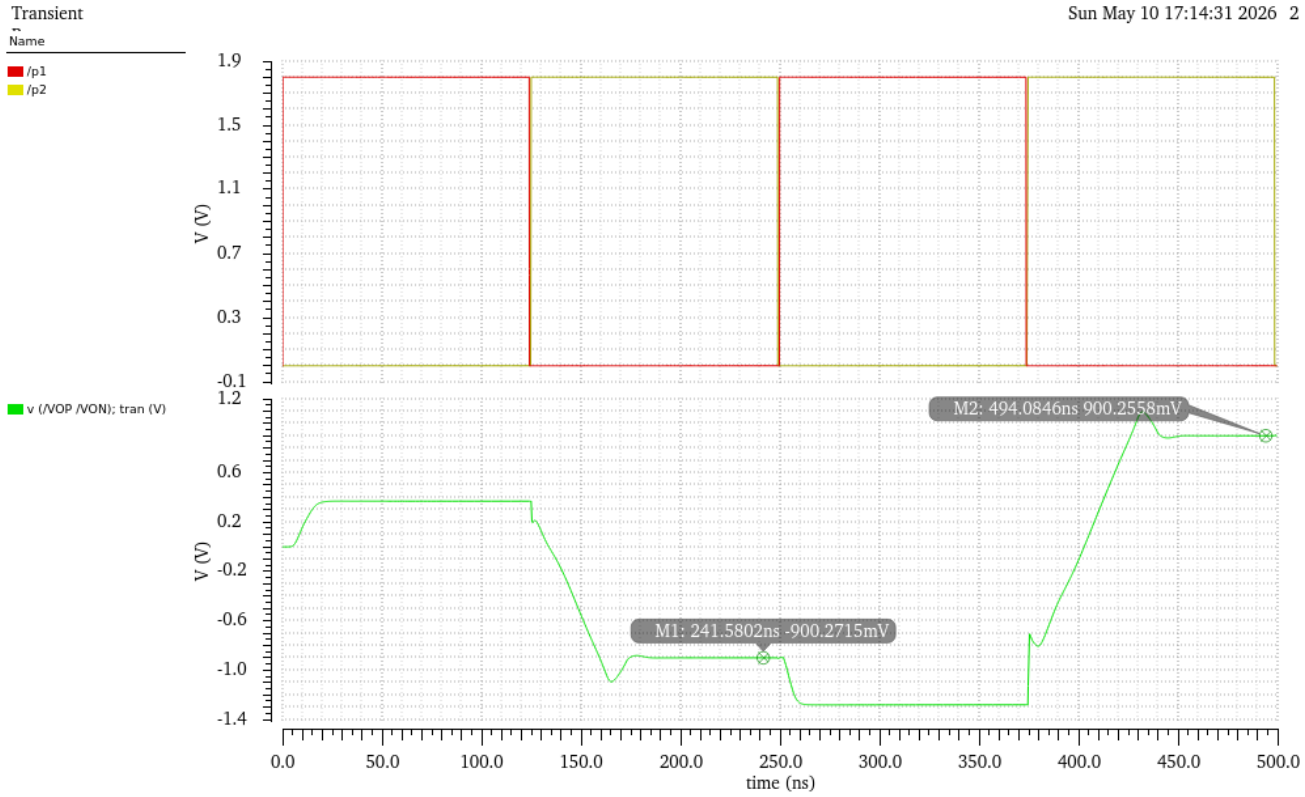


Fig. 15. Large-signal transient response of the complete switched-capacitor amplifier for a full-scale differential input transition from $+V_{FS}$ to $-V_{FS}$ and back to $+V_{FS}$, demonstrating stable settling and correct large-signal closed-loop operation.