Xingcan Chen

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EDUCATION

Columbia University — New York, NY
M.S. in Electrical Engineering — Sep 2025 - Present
Selected coursework: Advanced Logic Design, Embedded Systems, Advanced Digital Electronic Circuit, MOS Transistors.

University of Washington — Seattle, WA
B.S. in Electrical & Computer Engineering — Sep 2021 - Jun 2025
GPA: 3.68/4.00 | Dean's List: six quarters.

SELECTED ENGINEERING PROJECTS

1024-Point FFT Processor ASIC Design — Jan 2026 - May 2026
Columbia University | SystemVerilog, Synopsys DC/PT, Cadence Innovus, Python/NumPy

- Designed a radix-2 DIT FFT processor with Q1.15 arithmetic, a reusable butterfly datapath, a 512-entry twiddle ROM, and dual 1024 x 32-bit SRAM banks.
- Verified RTL, synthesized, and post-route netlists against NumPy references; achieved approximately 1.16% RMS-normalized NRMSE.
- Completed synthesis through routing and extraction in TSMC 65 nm, including SRAM integration and CTS; met the 100 MHz constraint with 5.48 ns setup and 0.19 ns hold slack in the clocked path group; achieved 3.70 MS/s effective throughput and generated GDSII, SPEF, and SDF.

Idaho Trail Embedded Game System — Jan 2026 - May 2026
Columbia University | DE1-SoC FPGA, SystemVerilog, C, Linux, Quartus Prime

- Built a 640 x 480 VGA controller with text, graphics, animation, and mode switching; implemented an 8 KB text buffer and dual 64 KB RGB332 framebuffers for double-buffered graphics.
- Integrated FPGA display hardware with Linux through Avalon-MM and device-driver access, then connected USB keyboard input and C game logic; debugged timing, addressing, and synchronization.
- Achieved a reported FMax of 99.19 MHz against a 50 MHz system clock requirement; integrated the final hardware demonstration.

64-Tap 16-Bit FIR Filter ASIC Design — Aug 2025 - Jan 2026
Columbia University | SystemVerilog, Synopsys DC/PT, MATLAB

- Implemented a sequential MAC datapath with Q1.15 inputs/coefficients, Q7.9 outputs, symmetric rounding, saturation, and FSM control for 10 kS/s input processing at a 100 MHz core clock.
- Added multi-flop synchronization and edge detection between input and processing clocks; completed RTL/gate-level simulation, synthesis, and STA in IBM 130 nm, reporting a 9.61 ns critical path, 0.00216 mm2 cell area, and 3.4 mW power.

INTERNSHIP EXPERIENCE

VisionX, LLC — San Jose, CA
Hardware Engineering Intern — Jul 2024 - Sep 2024

- Developed real-time vision applications on OpenNCC using Intel Movidius Myriad X VPU acceleration and OpenVINO, including skeleton tracking and gesture recognition.
- Independently built YOLOv3/v4 blind-spot detection for vehicles/pedestrians and Lucas-Kanade optical-flow video stabilization; collaborated on license plate detection and recognition.

RESEARCH EXPERIENCE

Real-Time Agentic Models for Smart Streetscapes — Summer 2026
Summer Research Project | New York, NY

- Research scope: agentic workflows for street-scene detection and weather understanding, workflow limitations, and the feasibility of local real-time inference across camera networks.

TECHNICAL SKILLS

Languages: SystemVerilog, Verilog, Python, C/C++, MATLAB.

Digital IC and FPGA: RTL and gate-level simulation, synthesis, STA, physical design; Design Compiler, PrimeTime, Innovus, Quartus Prime, Platform Designer.

Embedded and software: Embedded Linux, Avalon-MM, FPGA integration, Arduino, Git; OpenVINO, YOLOv3/v4, NumPy.

Communication: Mandarin Chinese (native), English (proficient).